

Compal confidential

JBK00 LA-4093P Schematics Document

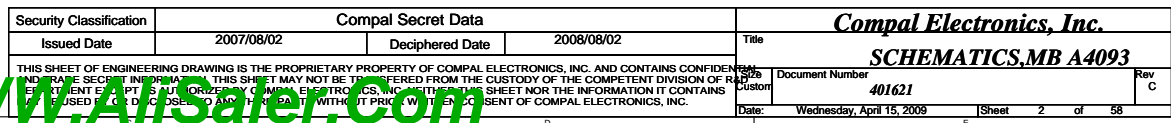
Mobile AMD S1G2 CPU with ATI
RX781 & SB700 core logic with M86-M

2009-03-25

REV:1.0

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Voltage Rails

power plane State	+B +3VL +5VL	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON X MEANS OFF

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010
ACCELEROMETER	3A	00111010

EC SM Bus1 address

EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	ADI1032-2 CPU	9AH	1001 101X b
24C16	A0H	1010 000X b	ADI1032-1 VGA	98H	1001 100X b
CPU SIC interface	98H	1001 100X b			

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

Layout Notes

@ : means just reserve , no build

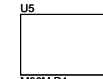
45@ : means need be mounted when 45 level assy or rework stage.

RX781R1@ : means just reserve for R1 FRU BOM

SBR1 @ : means just reserve for R1 FRU BOM

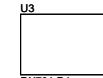
M86R1@ : means just reserve for R1 FRU BOM

M86M



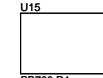
M86M R1
M86R3@

RX781



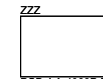
RX781 R1
RX781R3@

SB700



SB700 R1
SBR3@

PCB



PCB LA-4093P REV1.0 MB

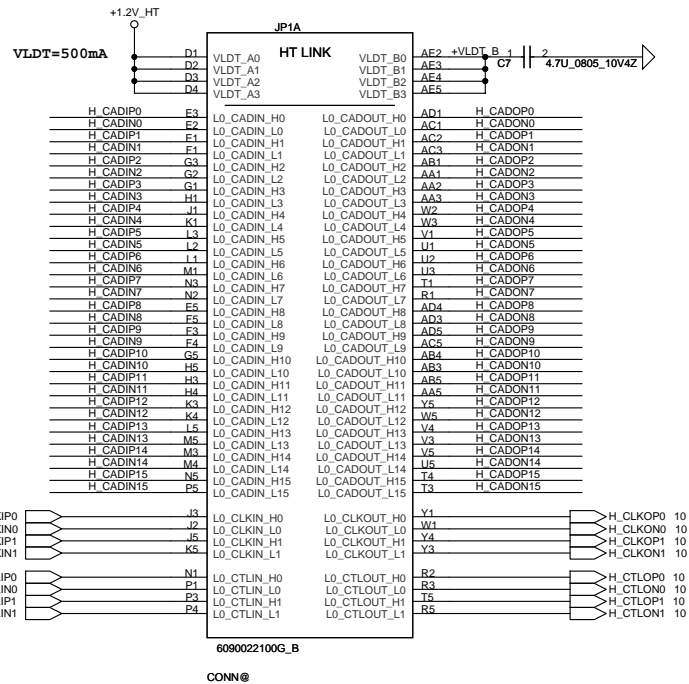
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK CHIP	MINI CARD Slot 2	LCD	HDMI	G-Sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X
I2C_CLK I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X
DDC_CLK0 DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X
DDC_CLK1 DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	X
SCL0 SDA0	SB700	X	X	X	X	V	V	X	X	X	V
SCL1 SDA1	SB700	X	X	X	X	X	X	V	X	X	X
SCL2 SDA2	SB700	X	X	X	X	X	X	X	X	X	X
SCL3 SDA3	SB700	X	X	X	X	X	X	X	X	X	X

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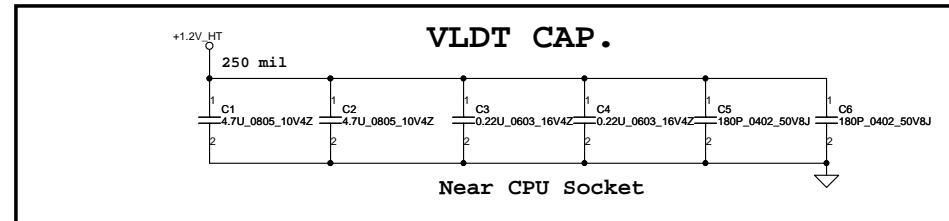
10 H_CADIP[0..15] H_CADIP[0..15]
10 H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] 10
H_CADON[0..15] H_CADON[0..15] 10

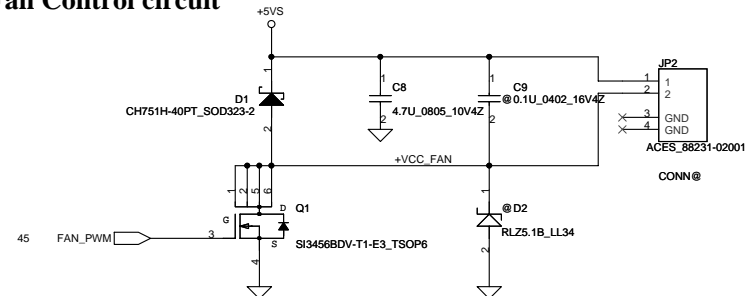


10 H_CLKIP0 J3 L0_CLKIN_H0 L0_CLKOUT_H0 Y1 H_CLKOP0 10
10 H_CLKIN0 J2 L0_CLKIN_L0 L0_CLKOUT_L0 W1 H_CLKON0 10
10 H_CLKIP1 J5 L0_CLKIN_H1 L0_CLKOUT_H1 Y4 H_CLKOP1 10
10 H_CLKIN1 K5 L0_CLKIN_L1 L0_CLKOUT_L1 Y3 H_CLKON1 10

10 H_CTLIP0 N1 L0_CTLIN_H0 L0_CTLOUT_H0 R2 H_CTLOP0 10
10 H_CTLIN0 P1 L0_CTLIN_L0 L0_CTLOUT_L0 R3 H_CTLON0 10
10 H_CTLIP1 P3 L0_CTLIN_H1 L0_CTLOUT_H1 T5 H_CTLOP1 10
10 H_CTLIN1 P4 L0_CTLIN_L1 L0_CTLOUT_L1 T6 H_CTLON1 10

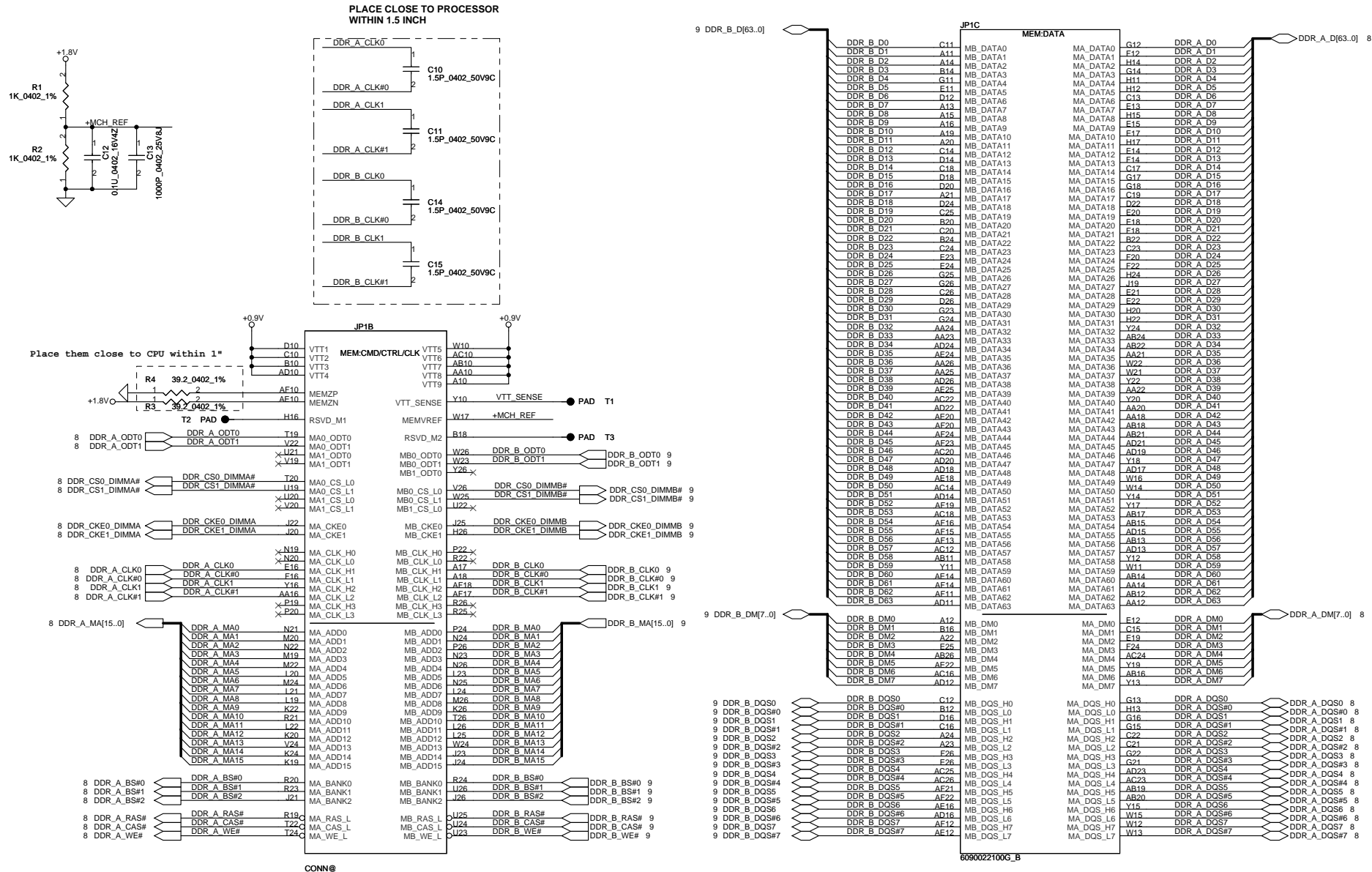


PWM Fan Control circuit

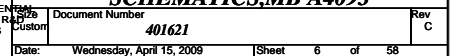


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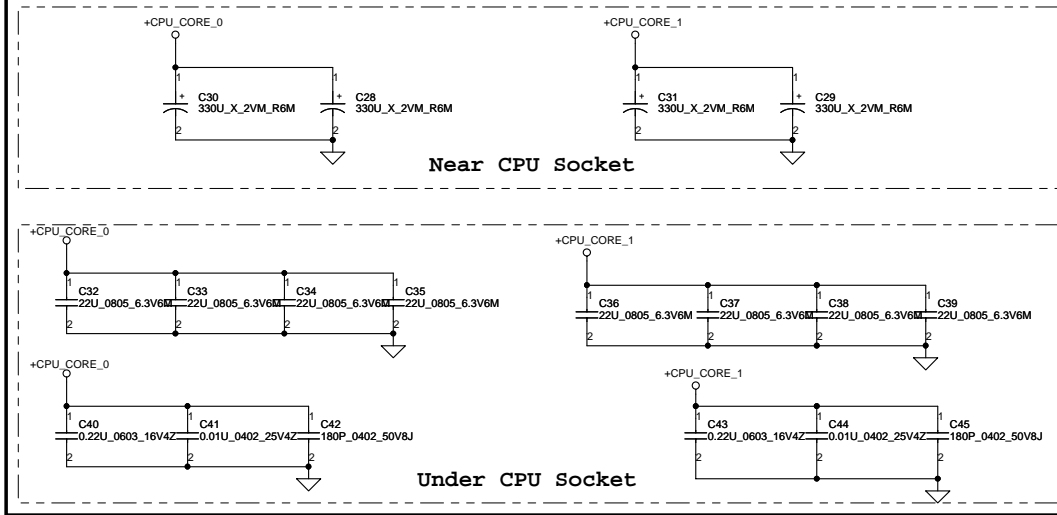
Processor DDR2 Memory Interface



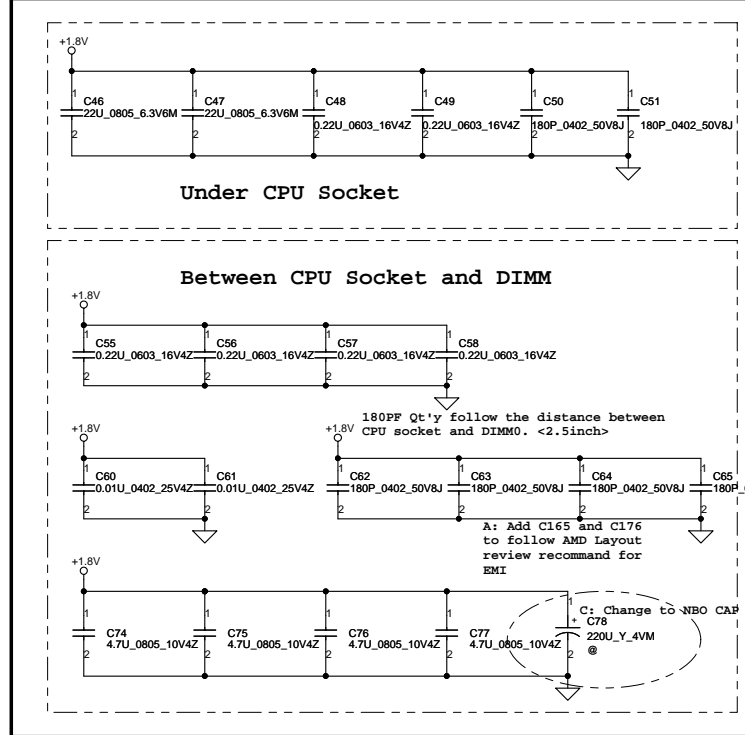
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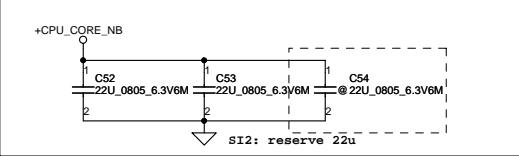
VDD(+CPU_CORE) decoupling.



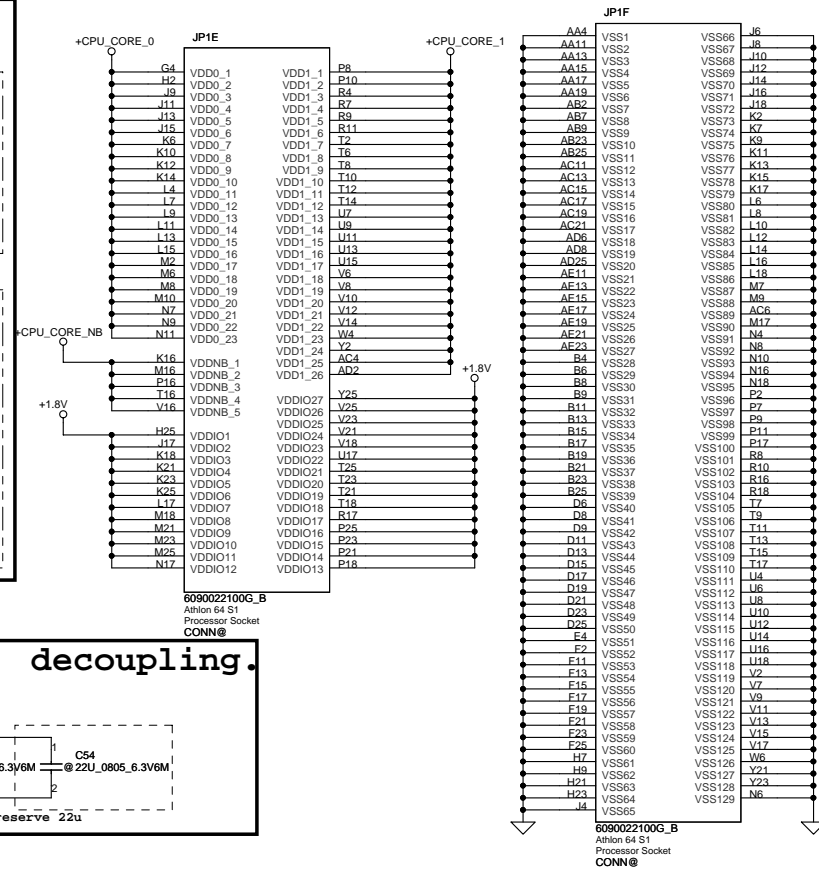
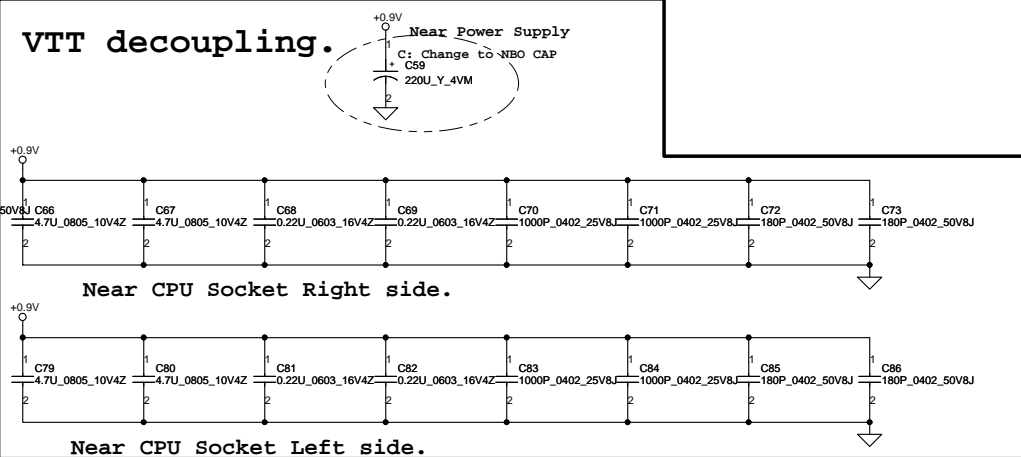
VDDIO decoupling.



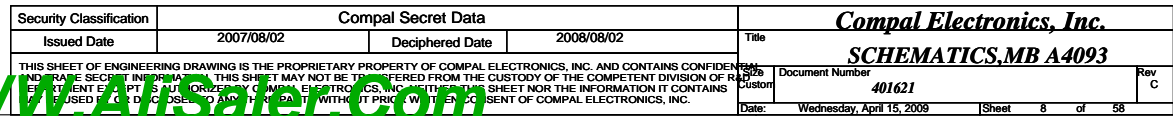
+CPU_CORE_NB decoupling.

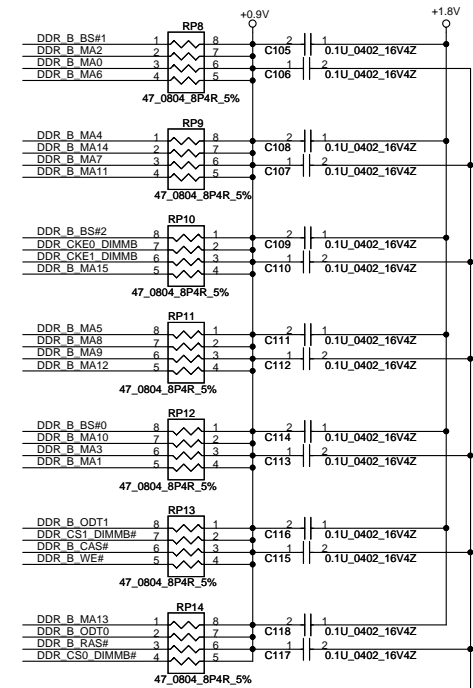


VTT decoupling.

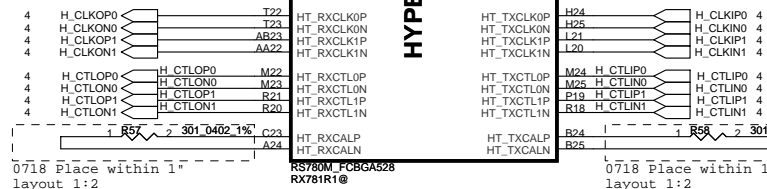
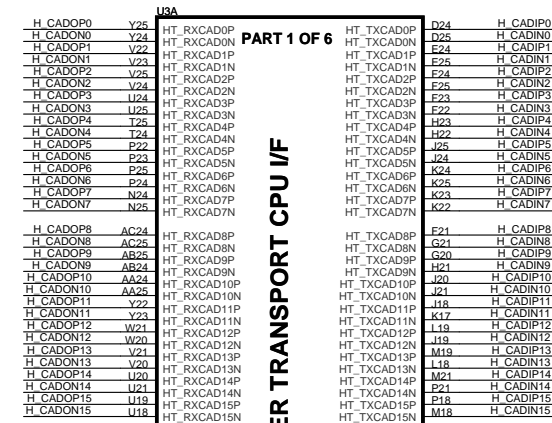
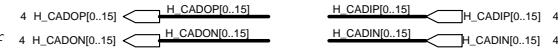
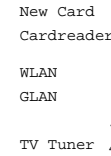
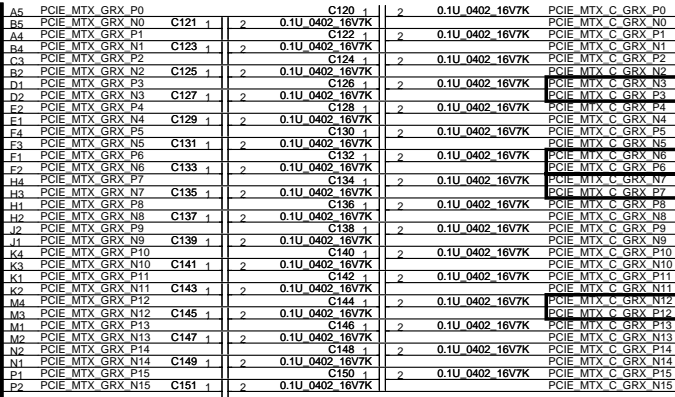
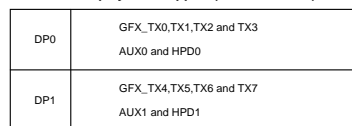
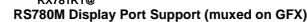
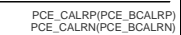
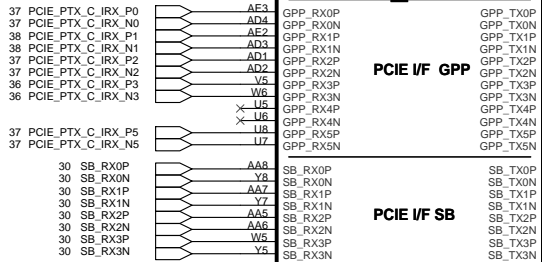
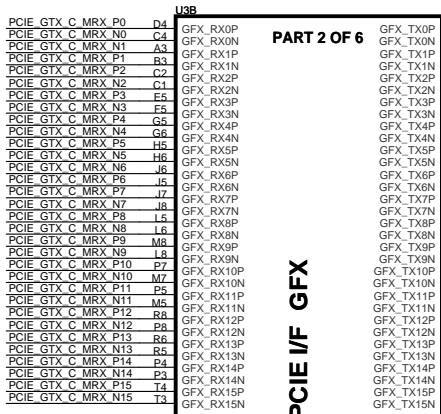
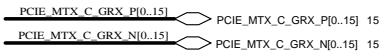


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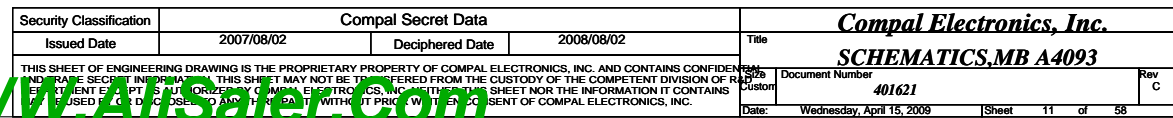


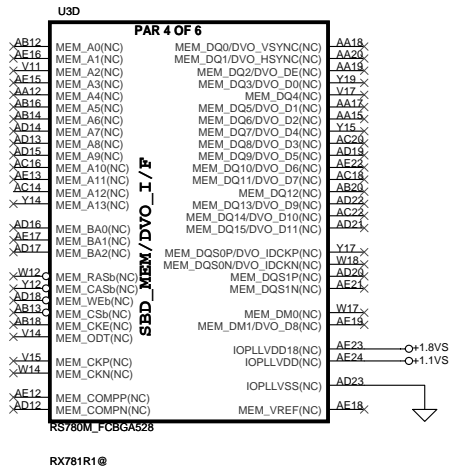


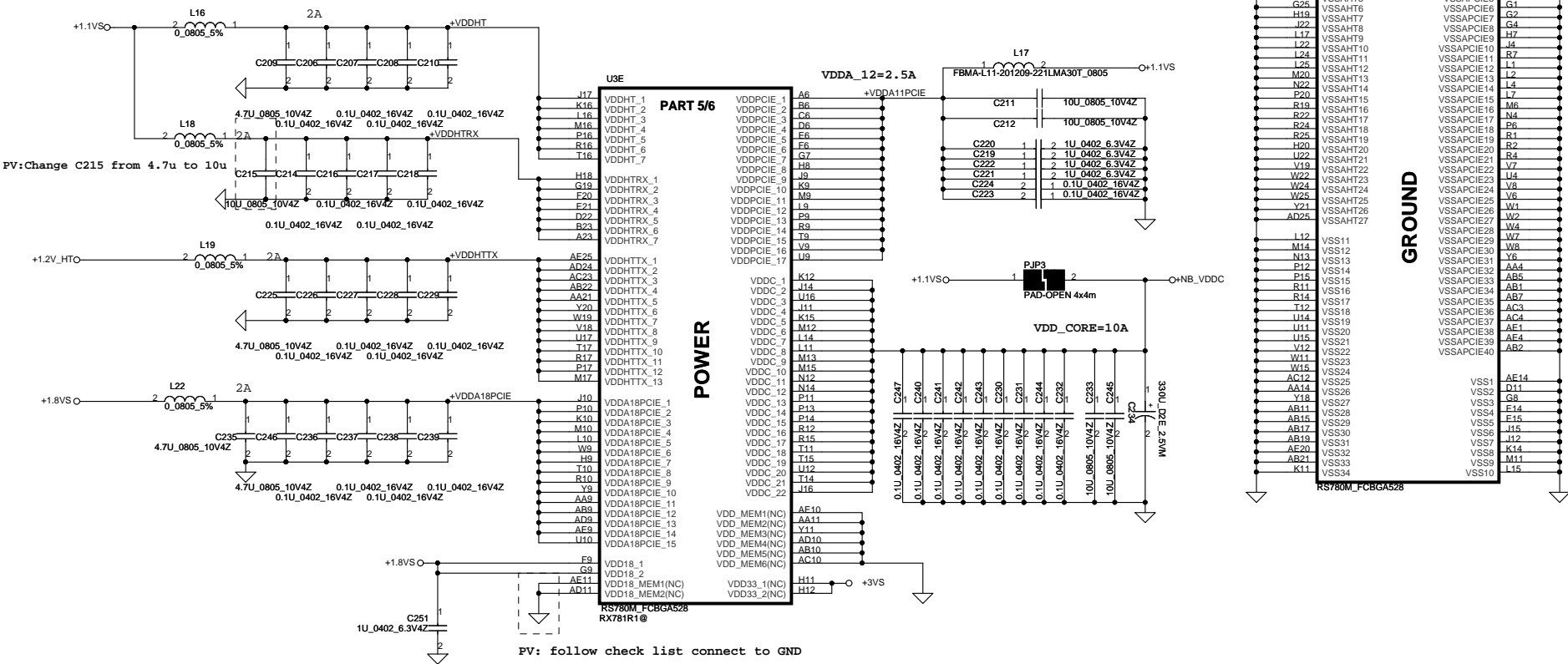
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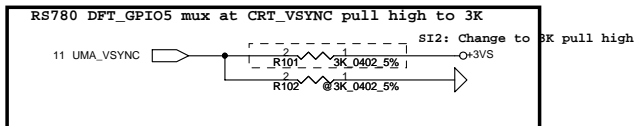
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DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

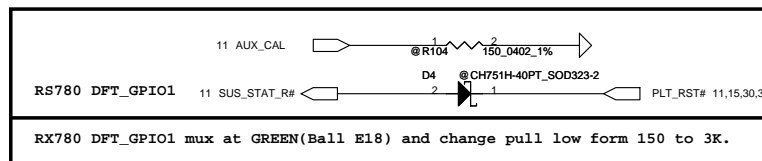
1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)
PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

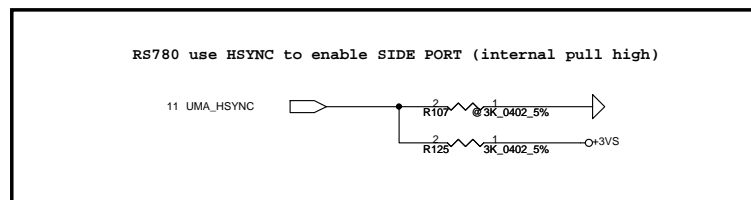
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

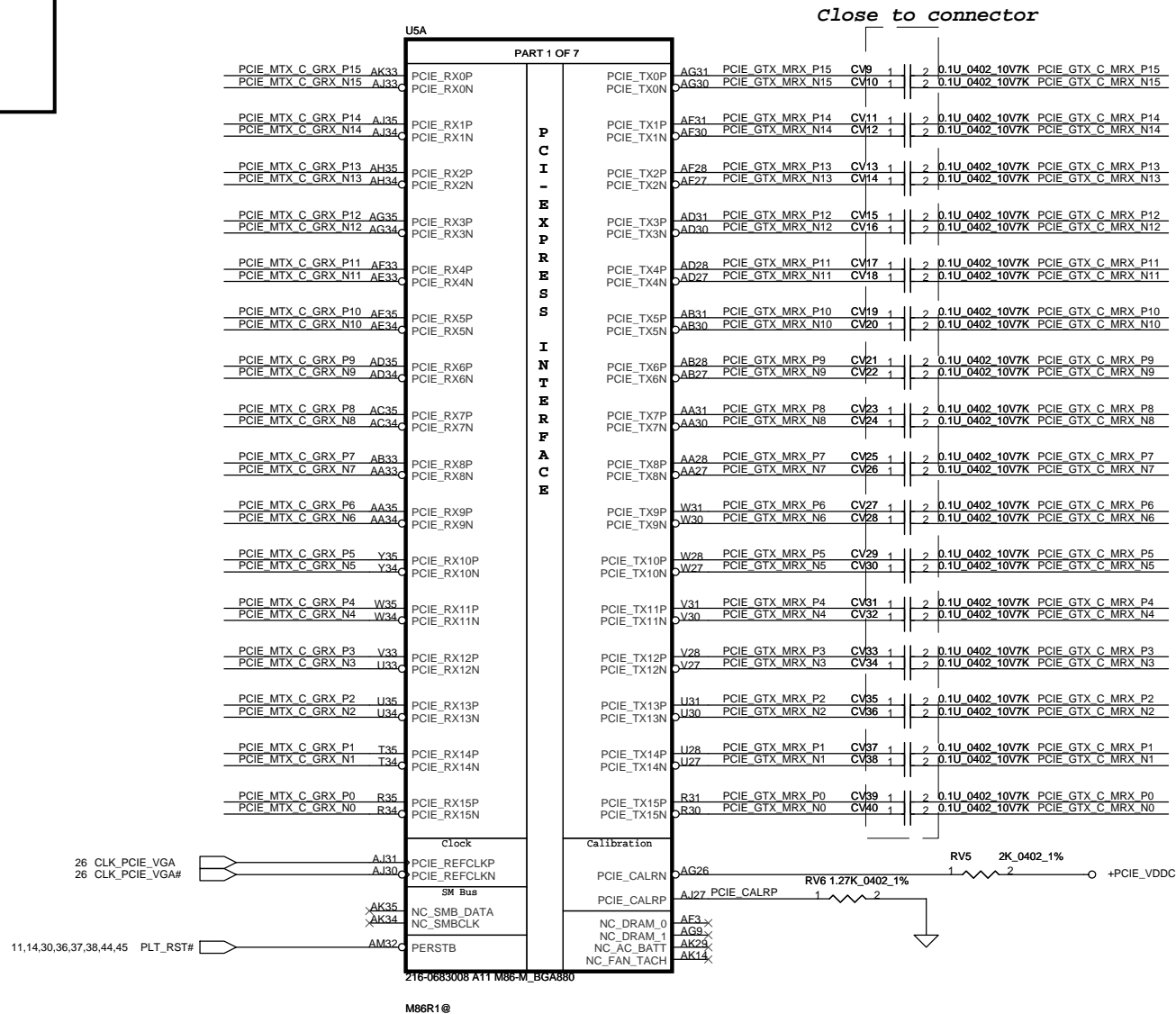
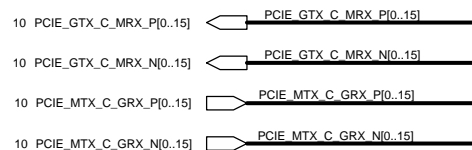
RX780: Enables the Test Debug Bus using PCIE bus

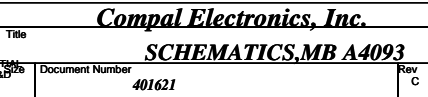
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

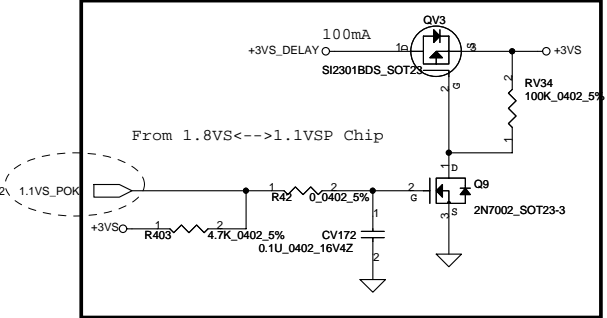
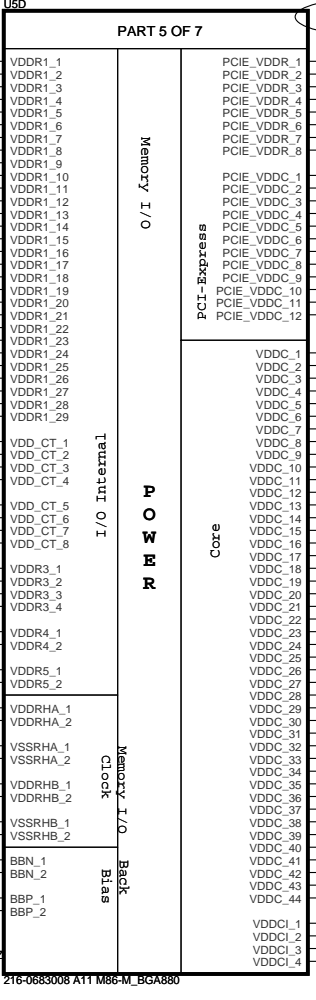
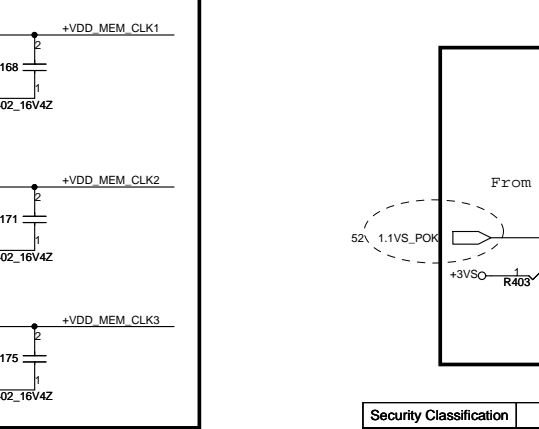
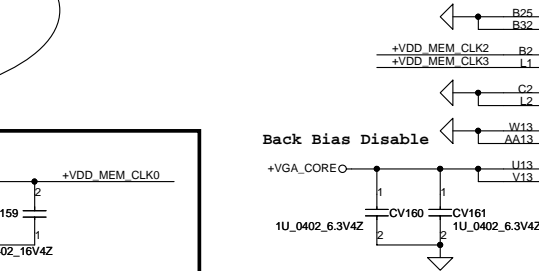
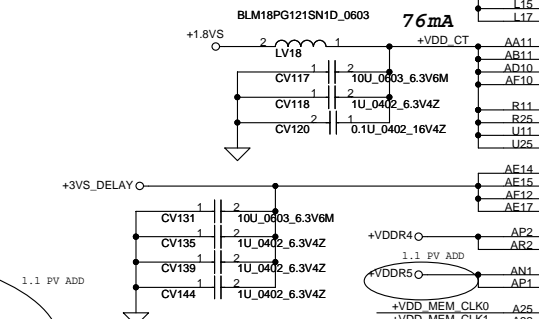
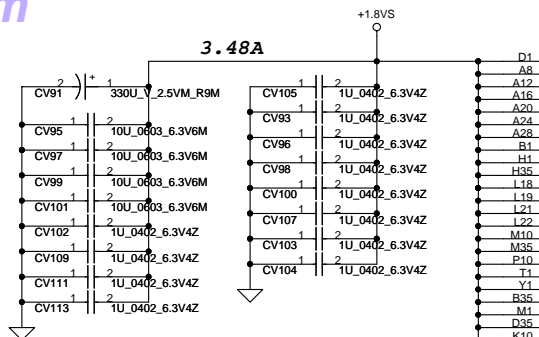
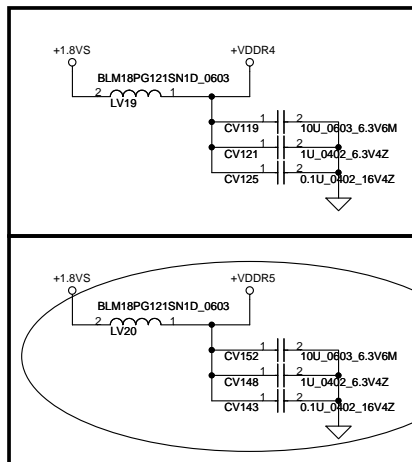
RS780: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS780)
0 : Enable (RS780)

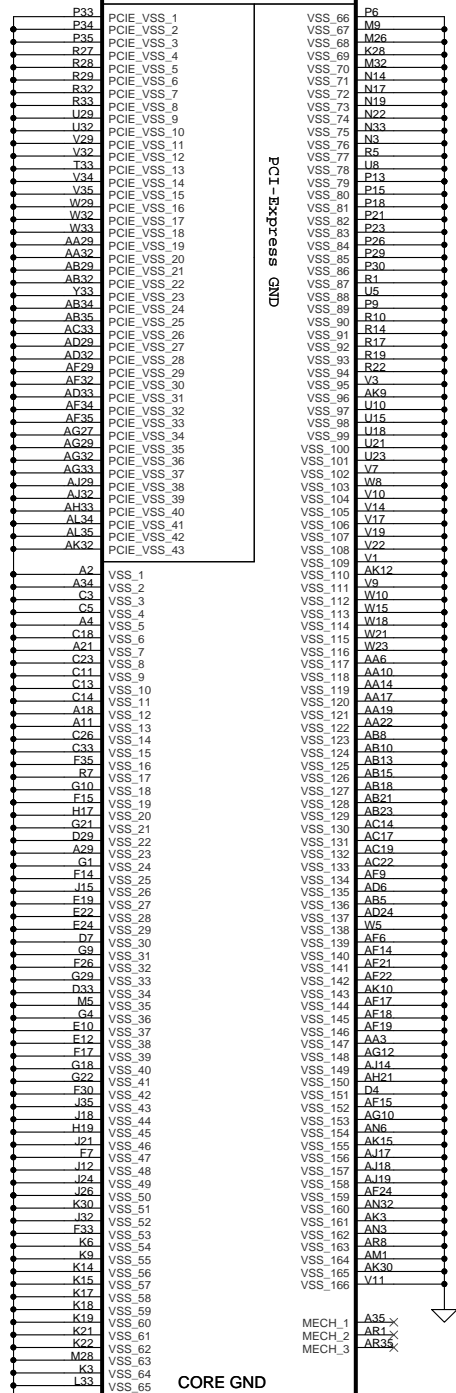
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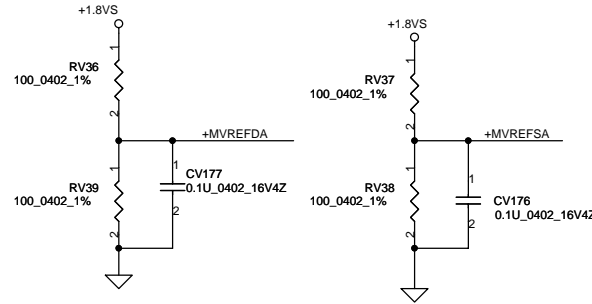
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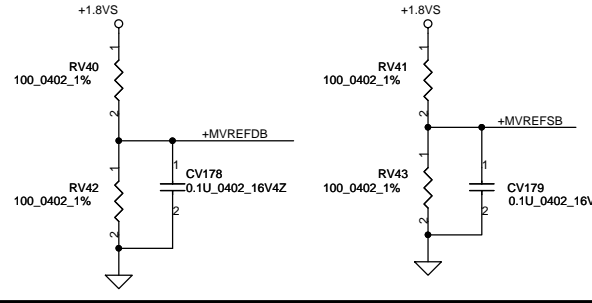
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DQMA#7..0]	<< DQMA#7..0]	21,22
QSA#7..0]	<< QSA#7..0]	21,22
QSA#7..0]	<< QSA#7..0]	21,22
MAA#12..0]	<< MAA#12..0]	21,22
BA#2..0]	<< BA#2..0]	21,22
MDA#63..0]	<< MDA#63..0]	21,22

Close to pin N34, N35



Close to pin A13, B14



MDB#63..0]	<< MDB#63..0]	23,24
MAB#12..0]	<< MAB#12..0]	23,24
BB#2..0]	<< BB#2..0]	23,24
DQMB#7..0]	<< DQMB#7..0]	23,24
QSB#7..0]	<< QSB#7..0]	23,24
QSB#7..0]	<< QSB#7..0]	23,24

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MEMORY INTERFACE A

write strobe read strobe

MDA0 P27	DQA_0	MAA_0	C27	MAA0
MDA1 P28	DQA_1	MAA_1	B28	MAA1
MDA2 P31	DQA_2	MAA_2	B27	MAA2
MDA3 P32	DQA_3	MAA_3	G26	MAA3
MDA4 M27	DQA_4	MAA_4	F27	MAA4
MDA5 K29	DQA_5	MAA_5	F27	MAA5
MDA6 K31	DQA_6	MAA_6	D27	MAA6
MDA7 K32	DQA_7	MAA_7	J27	MAA7
MDA8 M33	DQA_8	MAA_8	F29	MAA8
MDA9 M34	DQA_9	MAA_9	C30	MAA9
MDA10 L34	DQA_10	MAA_10	E26	MAA10
MDA11 L35	DQA_11	MAA_11	A27	MAA11
MDA12 J34	DQA_12	MAA_12	G27	MAA12
MDA13 J34	DQA_13	MAA_12	D26	BA2
MDA14 H33	DQA_14	MAA_BA2	C28	BA0
MDA15 H34	DQA_15	MAA_BA0	B29	BA1
MDA16 K27	DQA_16	MAA_BA1		
MDA17 J29	DQA_17			
MDA18 J30	DQA_18			
MDA19 J30	DQA_19			
MDA20 E29	DQA_20			
MDA21 F32	DQA_21			
MDA22 D30	DQA_22			
MDA23 D32	DQA_23			
MDA24 G33	DQA_24			
MDA25 G34	DQA_25			
MDA26 G35	DQA_26			
MDA27 F34	DQA_27			
MDA28 D34	DQA_28			
MDA29 C34	DQA_29			
MDA30 C35	DQA_30			
MDA31 B34	DQA_31			
MDA32 C24	DQA_32			
MDA33 B24	DQA_33			
MDA34 B23	DQA_34			
MDA35 A23	DQA_35			
MDA36 C21	DQA_36			
MDA37 B21	DQA_37			
MDA38 C20	DQA_38			
MDA39 B20	DQA_39			
MDA40 J22	DQA_40			
MDA41 H22	DQA_41			
MDA42 E22	DQA_42			
MDA43 D21	DQA_43			
MDA45 J19	DQA_44			
MDA46 F19	DQA_45			
MDA47 D19	DQA_46			
MDA48 C19	DQA_47			
MDA49 B19	DQA_48			
MDA50 A19	DQA_49			
MDA51 B18	DQA_50			
MDA52 C16	DQA_51			
MDA53 B16	DQA_52			
MDA54 C15	DQA_53			
MDA55 A15	DQA_54			
MDA56 H18	DQA_55			
MDA57 F18	DQA_56			
MDA58 E18	DQA_57			
MDA59 D18	DQA_58			
MDA60 J17	DQA_59			
MDA61 G15	DQA_60			
MDA62 F15	DQA_61			
MDA63 D15	DQA_62			

C31	<< ODTA0	21
C25	<< ODTA1	22
A33	<< CLKA0	21
A26	<< CLKA1	22
B33	<< CLKA0#	21
B26	<< CLKA1#	22
A31	<< RASA#0	21
D24	<< RASA#1	22
C32	<< CASA#0	21
H26	<< CASA#1	22
A30	<< CSA#0	21
B30	<< CSA#1	22
G24	<< CSA#1#	22
H24	<< CSA#1#	22
B31	<< CKEA0	21
F24	<< CKEA1	22
C29	<< WEA#0	21
D22	<< WEA#1	22

+MVREFDA N35
+MVREFSA N34

AM34

216-0683008 A11 M86-M_BGA880

M86R1@

U5G

Part 4 of 7

MEMORY INTERFACE B

MDB0 H15	DOB_0	MAB_0	H2	MAB0
MDB1 G14	DOB_1	MAB_1	H3	MAB1
MDB2 F14	DOB_2	MAB_2	J5	MAB2
MDB3 D14	DOB_3	MAB_3	J4	MAB3
MDB4 H12	DOB_4	MAB_4	J6	MAB4
MDB5 G12	DOB_5	MAB_5	J6	MAB5
MDB6 F12	DOB_6	MAB_6	G6	MAB6
MDB7 D10	DOB_7	MAB_7	J8	MAB7
MDB8 B13	DOB_8	MAB_8	F3	MAB8
MDB9 C12	DOB_9	MAB_9	F4	MAB9
MDB10 B12	DOB_10	MAB_10	J1	MAB10
MDB11 B11	DOB_11	MAB_11	J2	MAB11
MDB12 C9	DOB_12	MAB_12	J7	MAB12
MDB13 B9	DOB_13	MAB_12	F1	BB2
MDB14 A9	DOB_14	MAB_BA2	G2	BB0
MDB15 B8	DOB_15	MAB_BA0	G3	BB1
MDB16 J10	DOB_16	MAB_BA1		
MDB17 H10	DOB_17			
MDB18 F10	DOB_18			
MDB19 D9	DOB_19			
MDB20 G7	DOB_20			
MDB21 G6	DOB_21			
MDB22 F6	DOB_22			
MDB23 D6	DOB_23			
MDB24 C8	DOB_24			
MDB25 C7	DOB_25			
MDB26 B7	DOB_26			
MDB27 A7	DOB_27			
MDB28 B5	DOB_28			
MDB29 A5	DOB_29			
MDB30 C4	DOB_30			
MDB31 B4	DOB_31			
MDB32 M3	DOB_32			
MDB33 M2	DOB_33			
MDB34 N2	DOB_34			
MDB35 M1	DOB_35			
MDB36 R3	DOB_36			
MDB37 R2	DOB_37			
MDB38 T3	DOB_38			
MDB39 T2	DOB_39			
MDB40 M8	DOB_40			
MDB41 M7	DOB_41			
MDB42 P5	DOB_42			
MDB43 P4	DOB_43			
MDB44 R9	DOB_44			
MDB45 R8	DOB_45			
MDB46 R6	DOB_46			
MDB47 U4	DOB_47			
MDB48 U3	DOB_48			
MDB49 U2	DOB_49			
MDB50 U1	DOB_50			
MDB51 V2	DOB_51			
MDB52 Y3	DOB_52			
MDB53 Y2	DOB_53			
MDB54 A4	DOB_54			
MDB55 U9	DOB_55			
MDB57 U7	DOB_56			
MDB58 U6	DOB_57			
MDB59 V4	DOB_58			
MDB60 W9	DOB_59			
MDB61 W7	DOB_60			
MDB62 W6	DOB_61			
MDB63 V4	DOB_62			
	DOB_63			

+MVREFDB B14

+MVREFSB A13

TESTEN

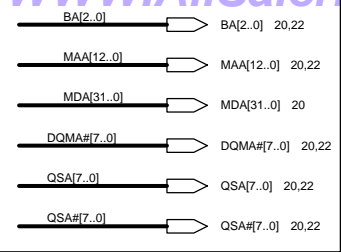
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TEST_YCLK

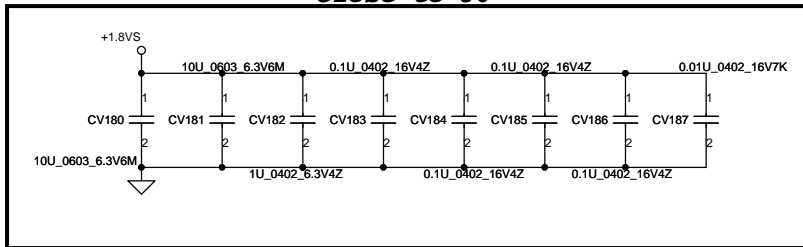
MEMTEST

PLLTEST

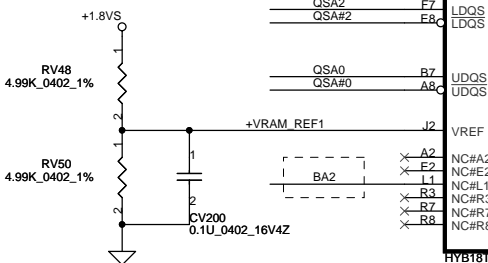
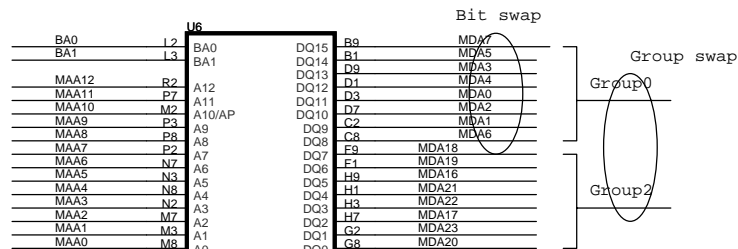
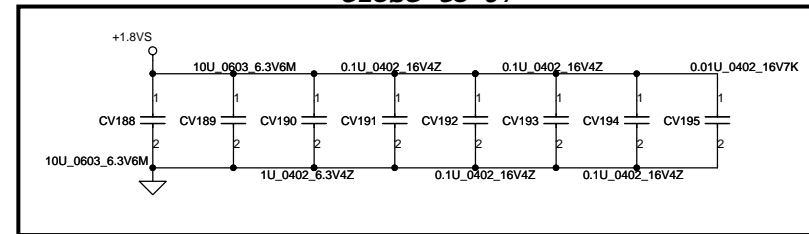
216-0683008 A11 M86-M_BGA880



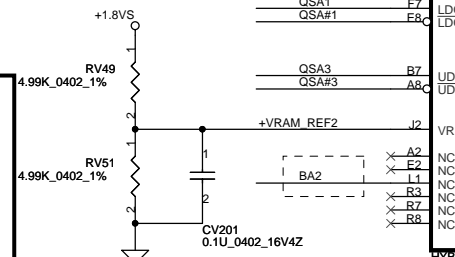
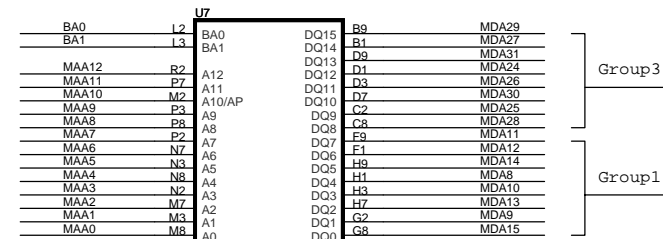
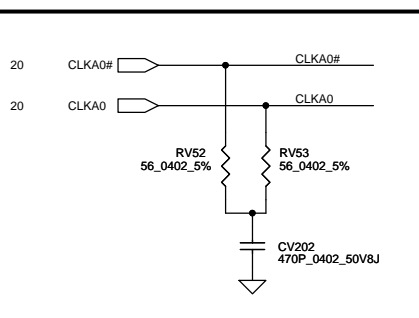
Close to U6



Close to U7



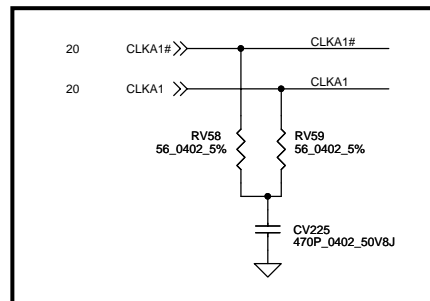
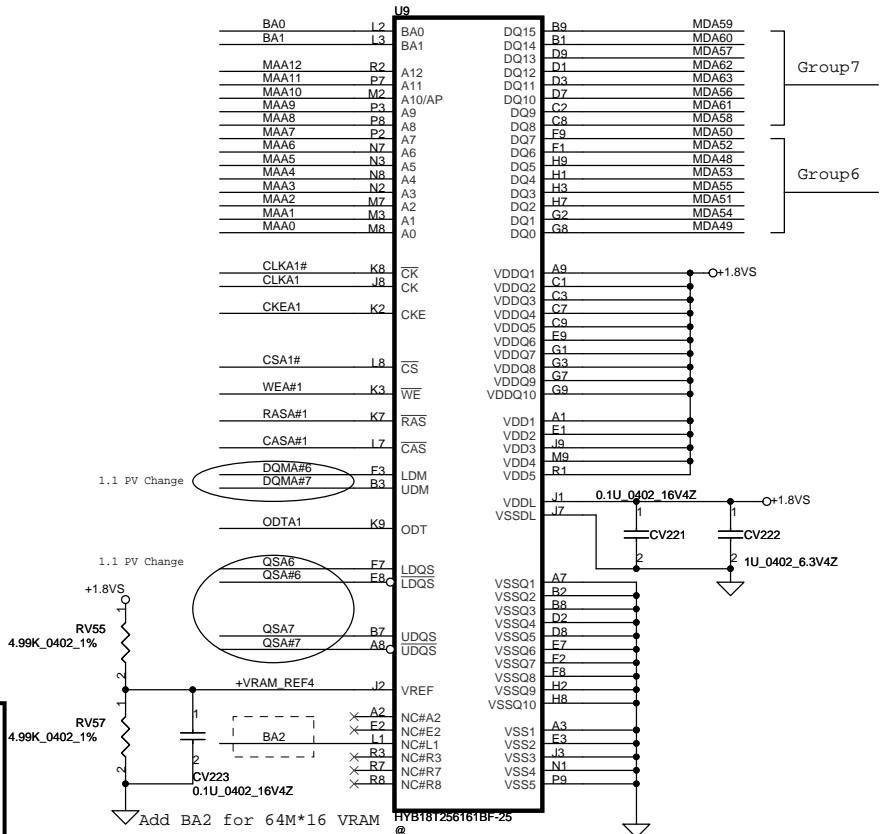
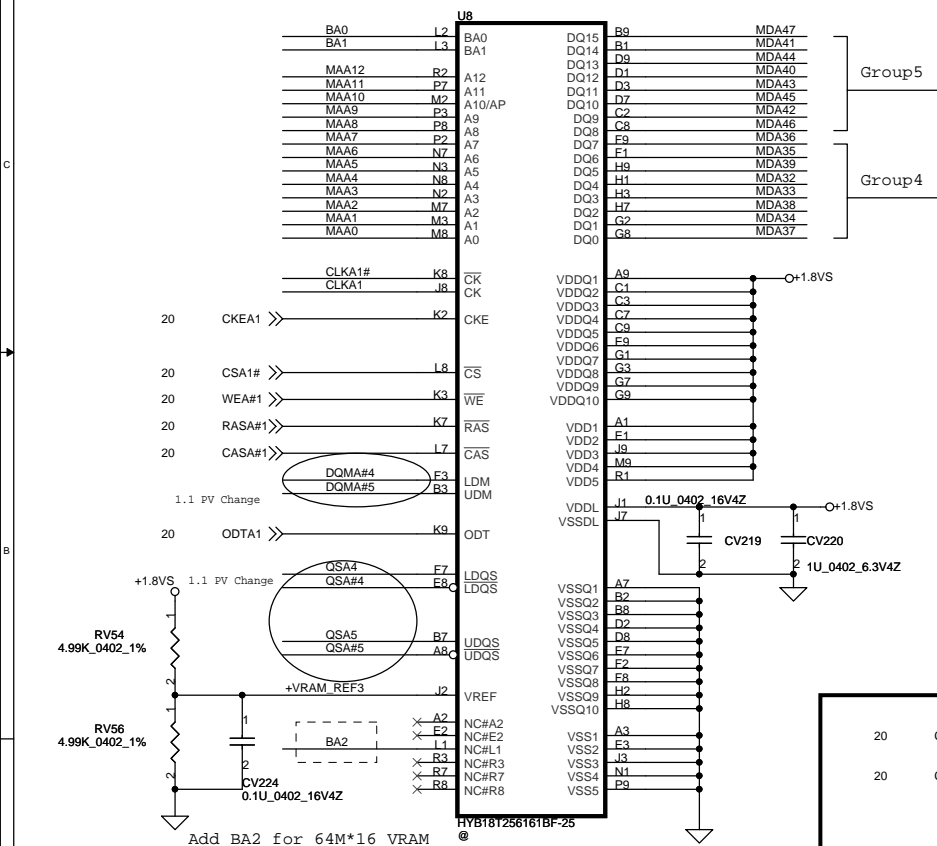
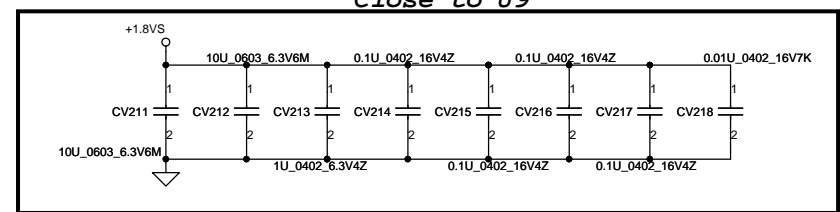
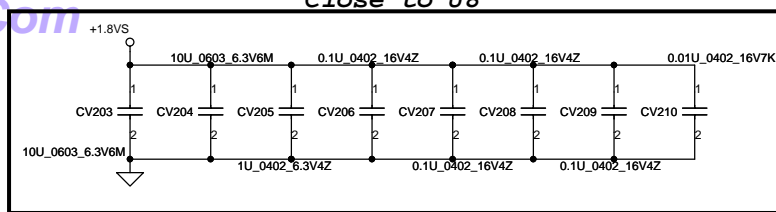
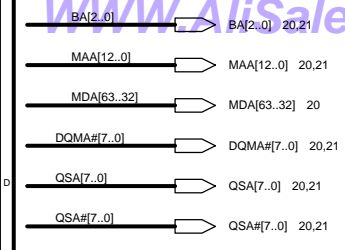
Add BA2 for 64M*16 VRAM



Add BA2 for 64M*16 VRAM

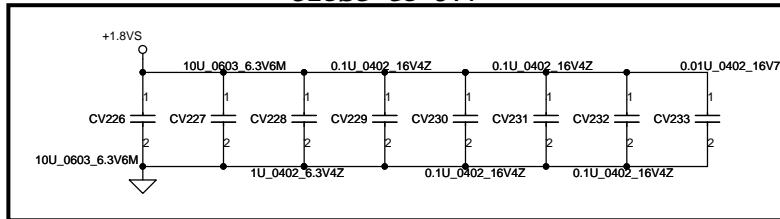
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Date				Wednesday, April 15, 2009	Sheet 21 of 58

Close to U9

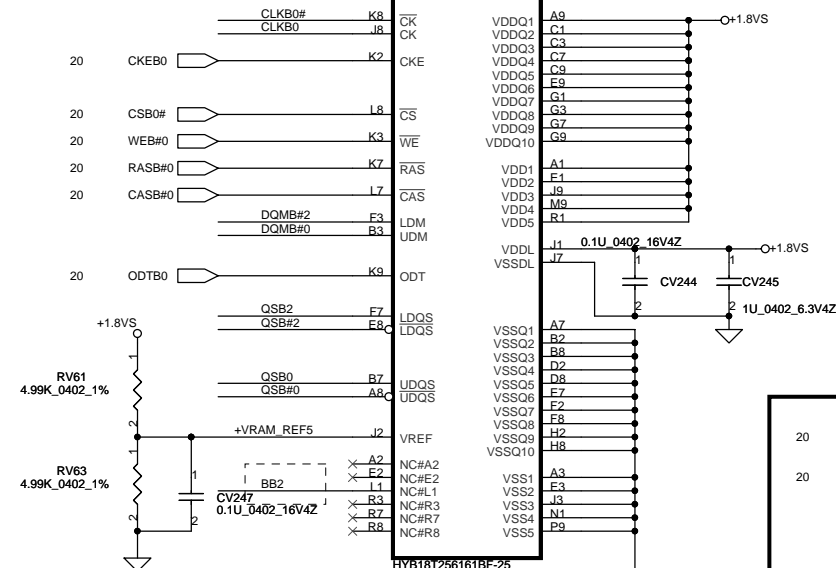
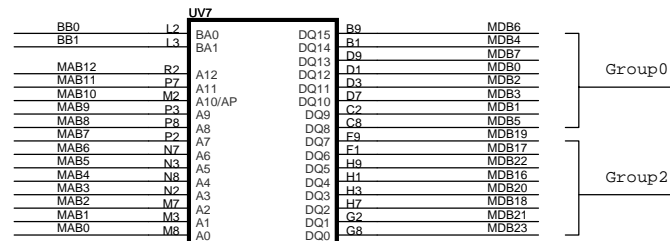
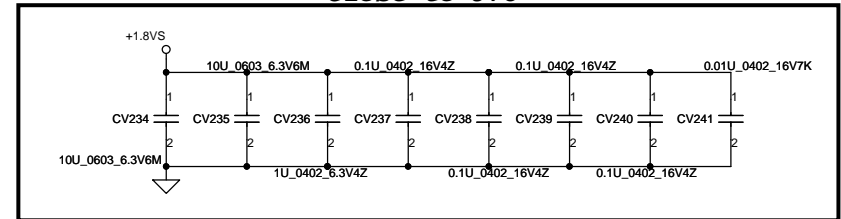


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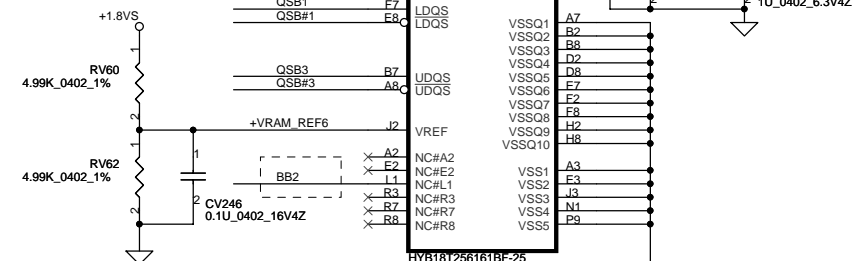
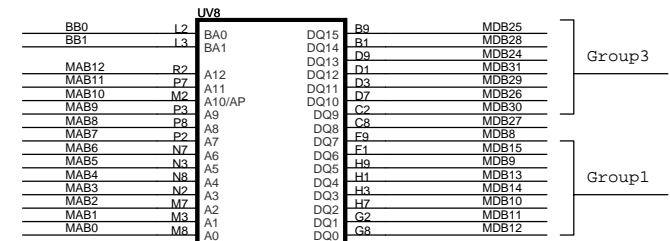
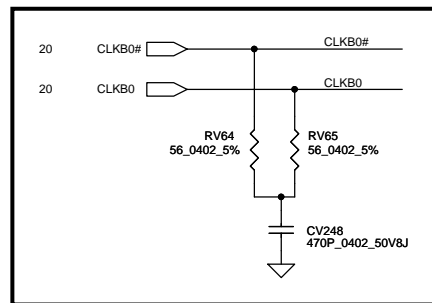
Close to UV7



Close to UV8



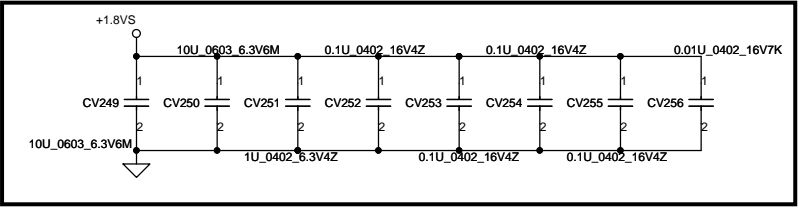
Add BA2 for 64M*16 VRAM



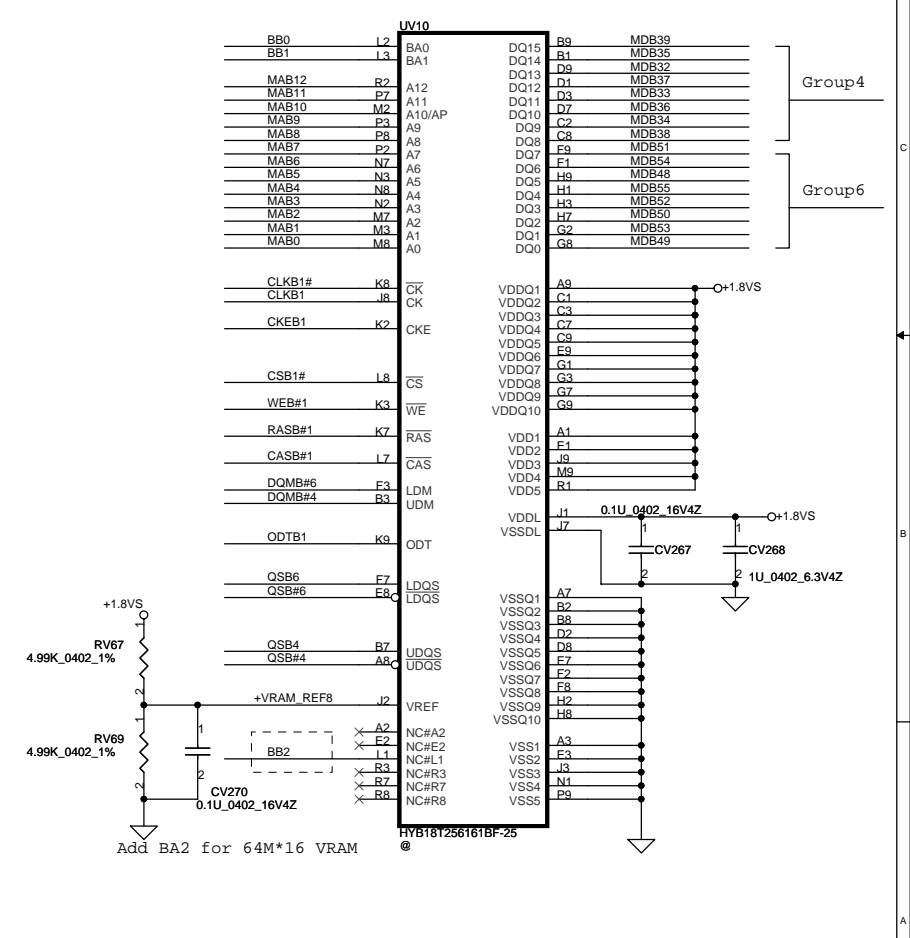
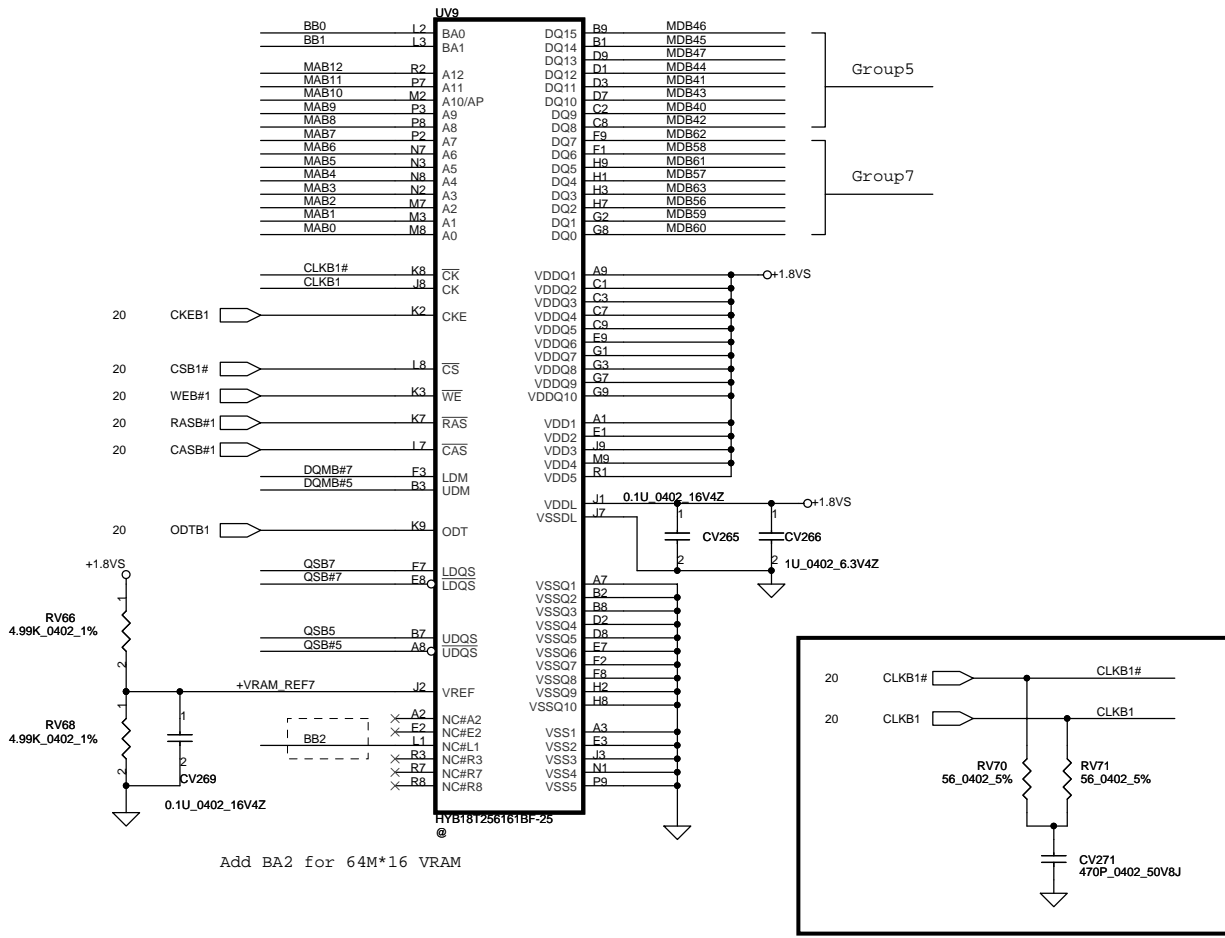
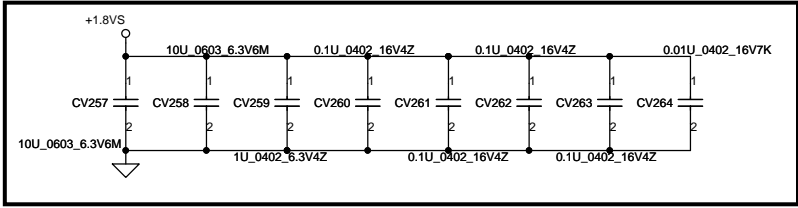
Add BA2 for 64M*16 VRAM

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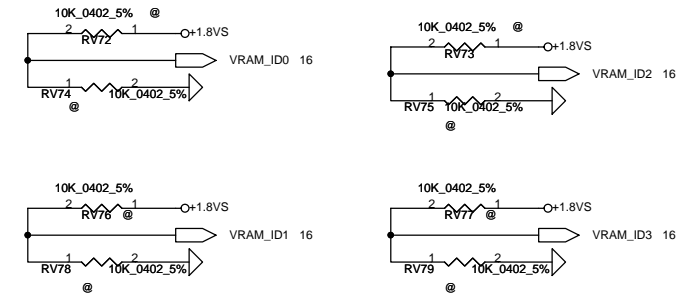
Close to UV9



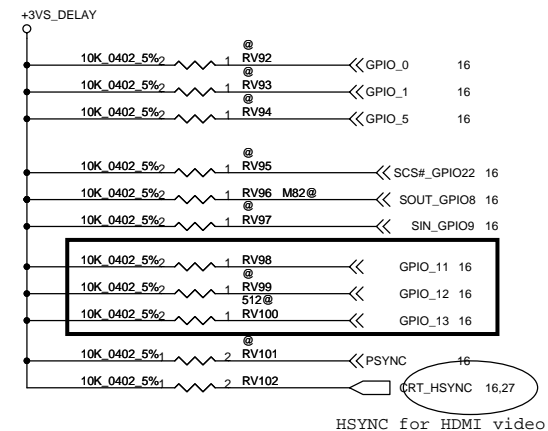
Close to UV10



STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M82M-XT	JBK00 1.0a	512M(x4)	Samsung 64Mx16 1.8V	SA00002MD00	0 0 0 0
			JBK00 1.0	256M(X4)	Samsung 32Mx16 1.8V	SA00002AJ10	0 0 0 1
				512M(x4)	Hynix 64Mx16 1.8V		0 0 1 0
			JBK00 1.0	256M(X4)	Hynix 32Mx16 1.8V	SA00002DL00	0 0 1 1
			JBK00 1.0	256M(X4)	Qimonda 32Mx16 1.8V	SA00002A600	0 1 0 0
			JBK00 1.0a	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF00	0 1 0 1
		M86M	JBK00 1.1	512M(x8)	Samsung 32Mx16 1.8V	SA00002AJ10	0 1 1 0
			JBK00 1.1	512M(x8)	Hynix 32Mx16 1.8V	SA00002DL00	0 1 1 1
			JBK00 1.1	512M(x8)	Qimonda 32Mx16 1.8V	SA00002A600	1 0 0 0
				1G(x8)	Samsung 64Mx16 1.8V	SA00002MD00	1 0 0 1
				1G(x8)	Hynix 64Mx16 1.8V		1 0 1 0
				1G(x8)	Qimonda 64Mx16 1.8V	SA00002MF00	1 0 1 1

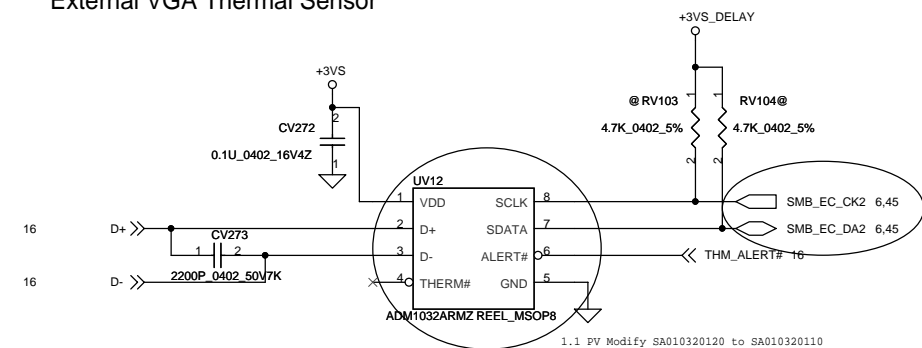


STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED M8X
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO M86-M ONLY	
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO M82-M ONLY	
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 0 1
BIF_VGA_DIS	PSYNC	VGA ENABLED===0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1

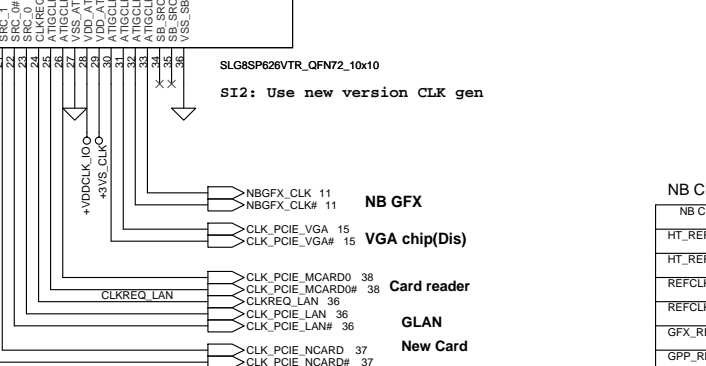
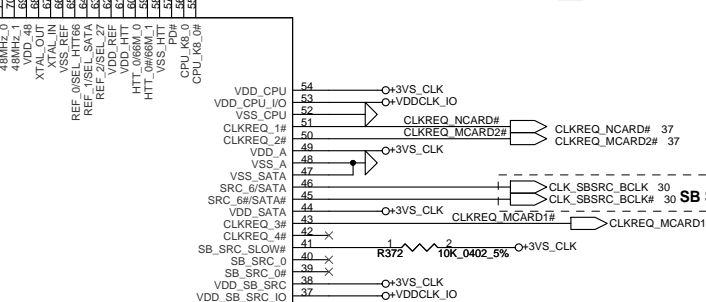
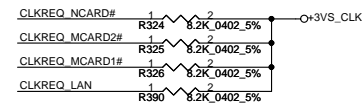
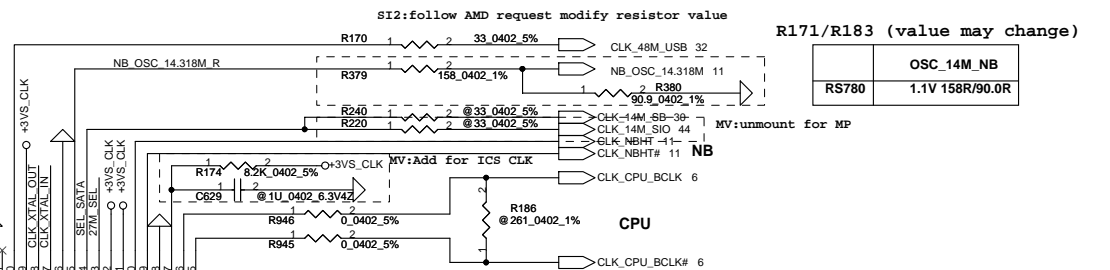
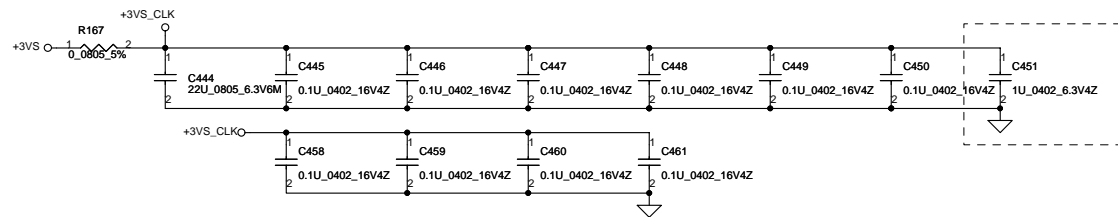


GPIO9 = 0 (BIOS_ROM_EN = 0)	
GPIO[13:11]	MEMORY SIZE
0 0 0	128MB
0 0 1	256MB
0 1 0	64MB
1 0 0	512MB

External VGA Thermal Sensor



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NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P		
REFCLK_N	14M SE (1.8V) NC	14M SE (1.1V) vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTP
GPPSB_REFCLK	100M DIFF	100M DIFF

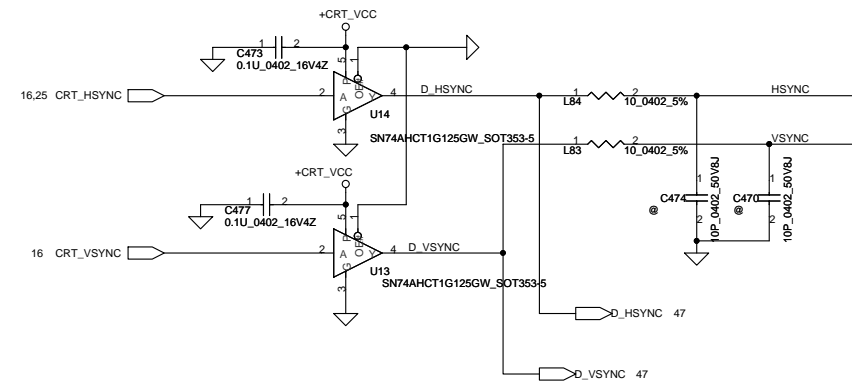
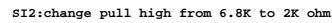
27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC 7 output

* default

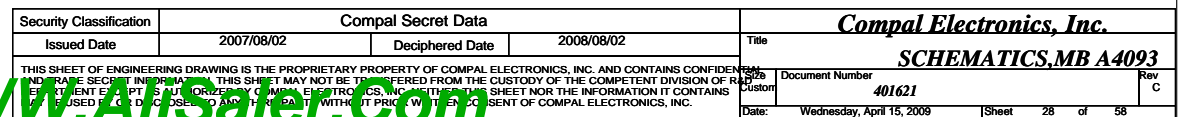
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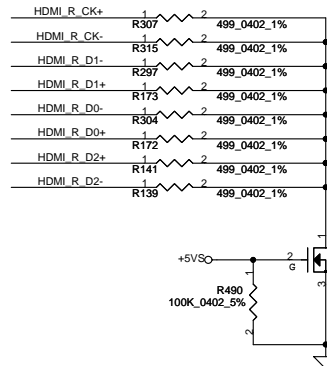
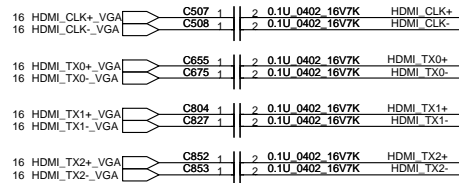
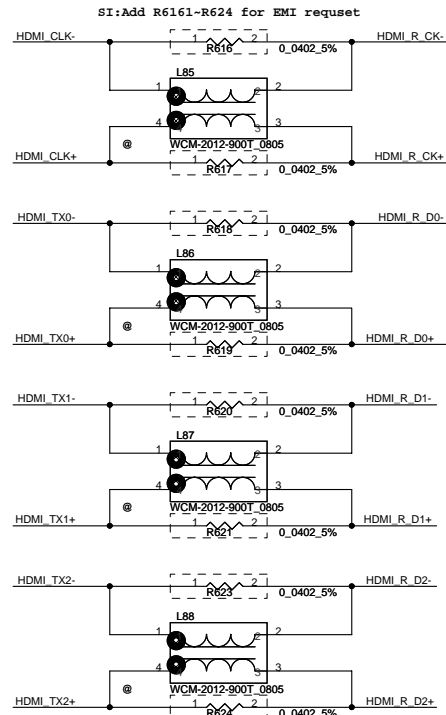
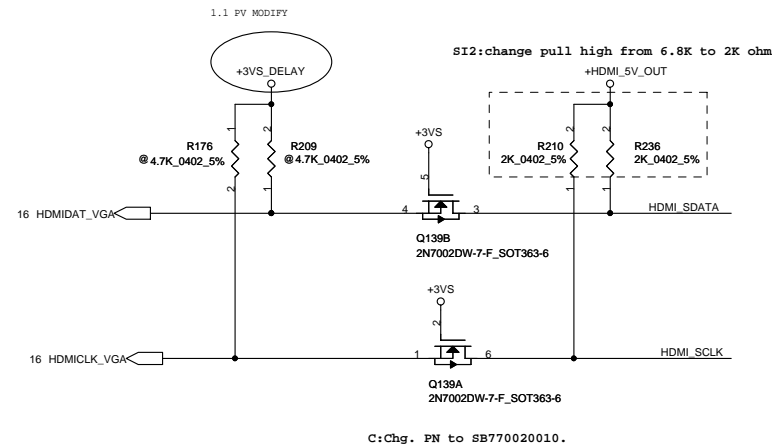
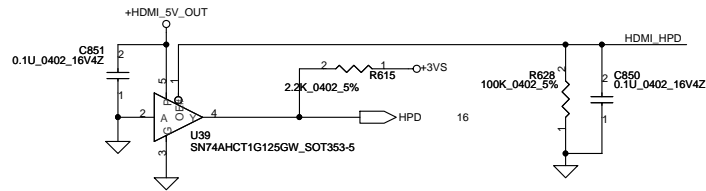
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Title			
SCHEMATICS, MB A4093			
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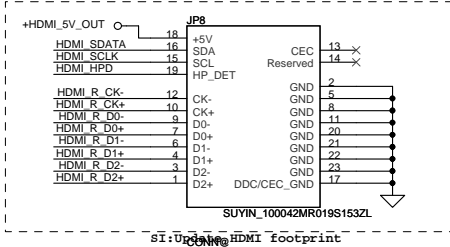


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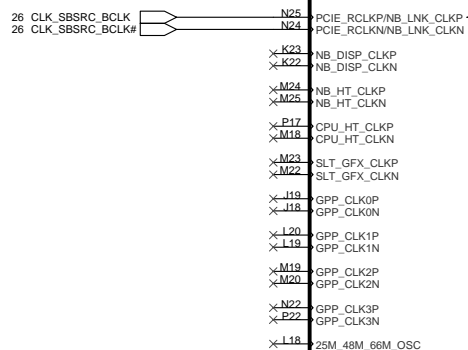
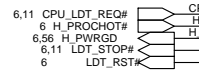
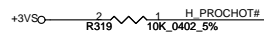
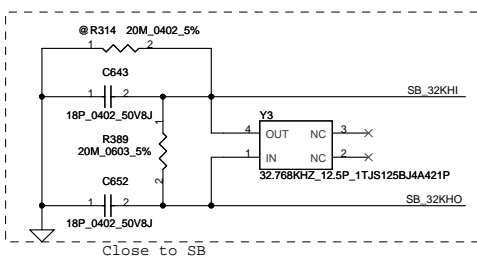
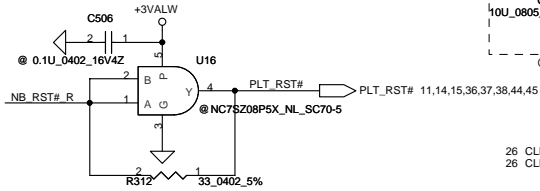
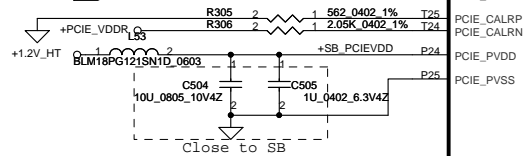
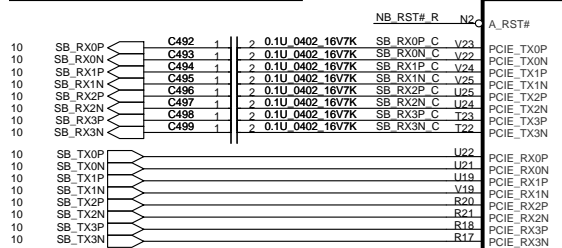
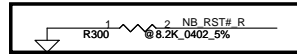


HDMI Connector



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Check AMD need pull low or not



218S7EALA11FG_BGA528_SB700

SB700

Part 1 of 5

PCI EXPRESS INTERFACE

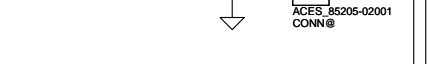
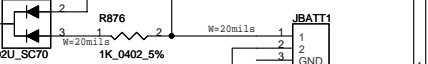
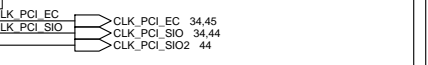
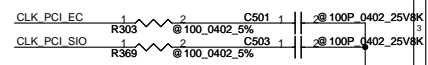
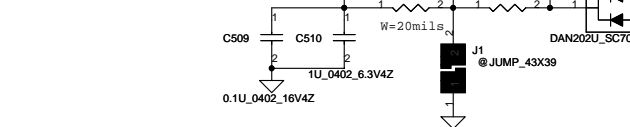
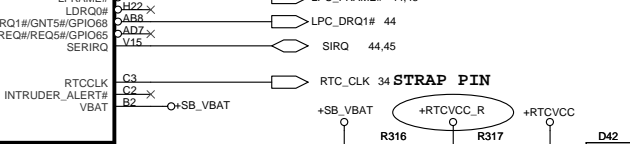
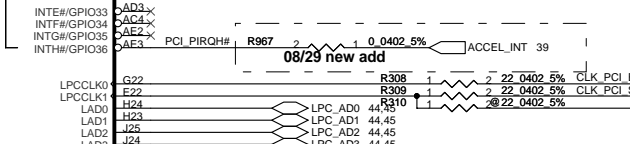
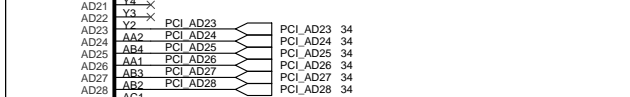
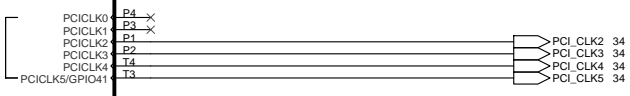
PCI INTERFACE

CLOCK GENERATOR

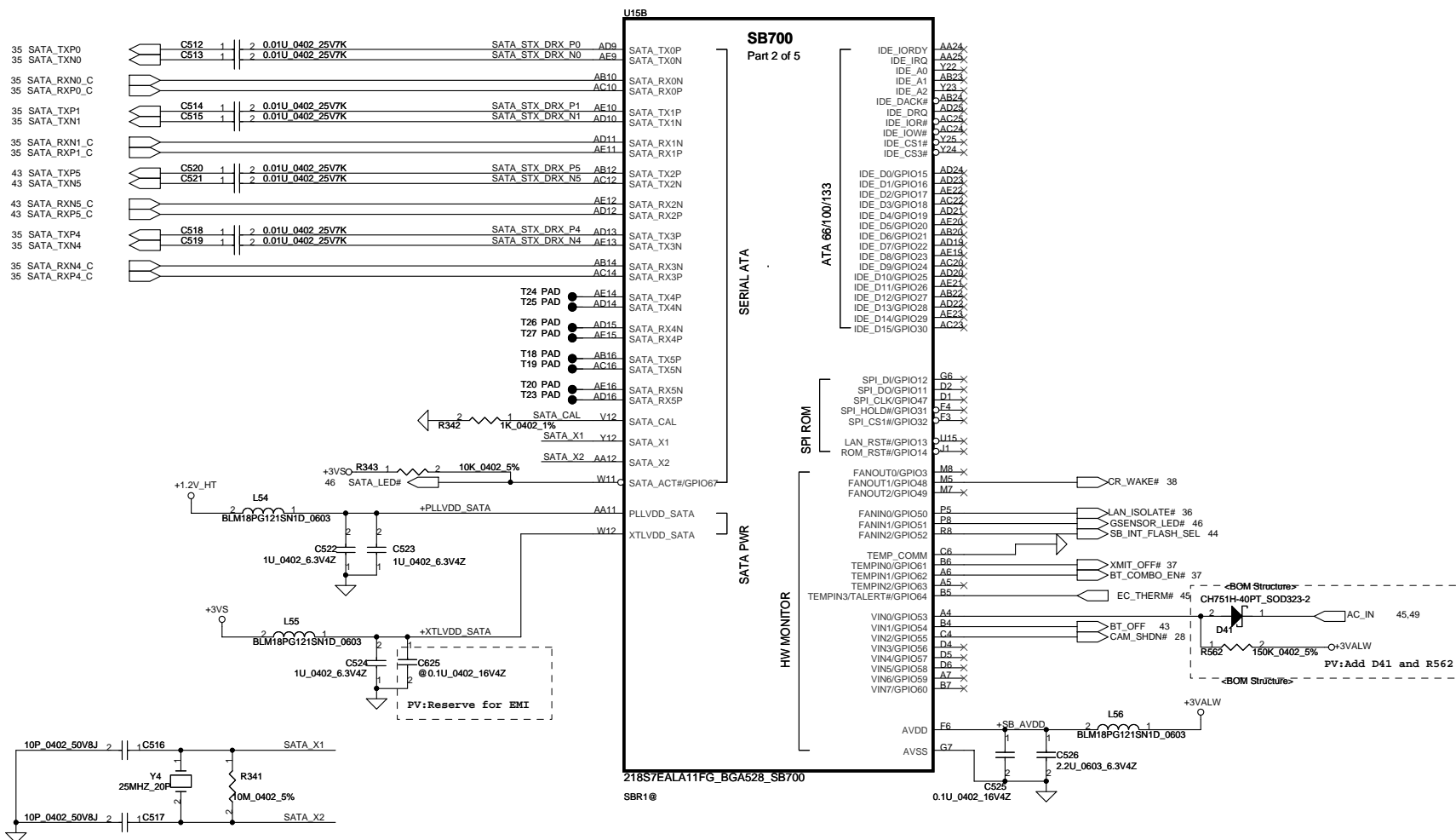
LPC

RTC XTAL

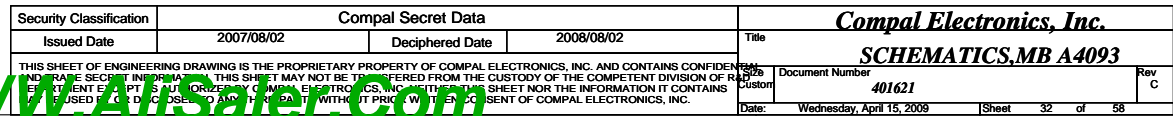
CPU

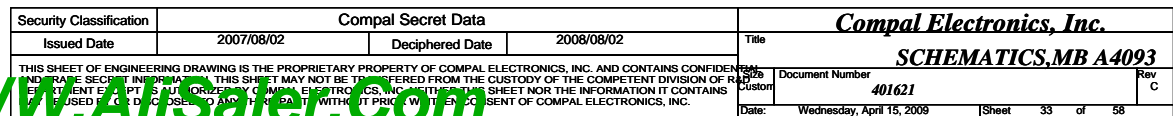


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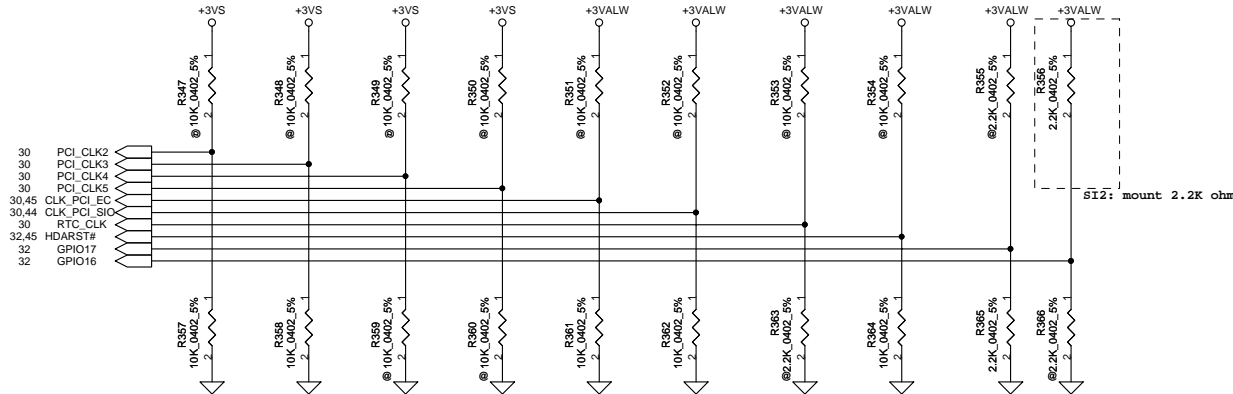




REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

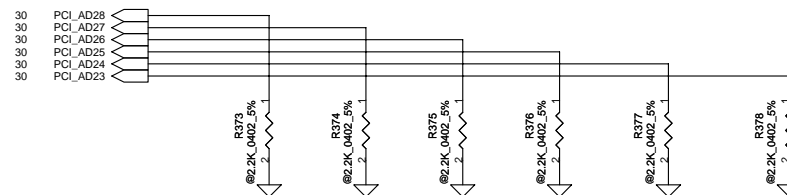
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

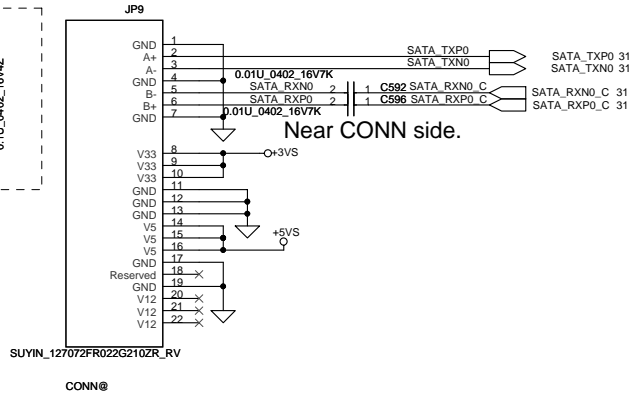
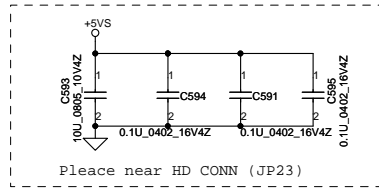
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

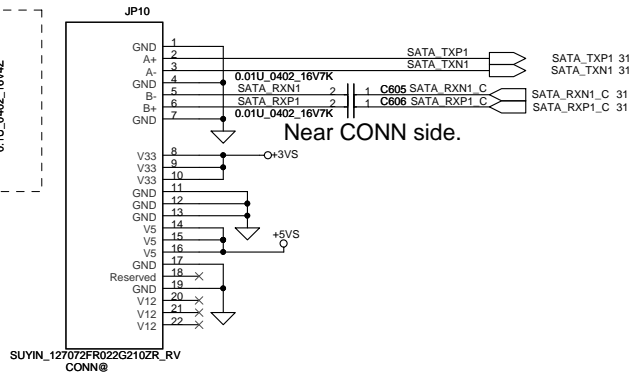
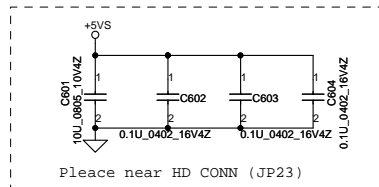


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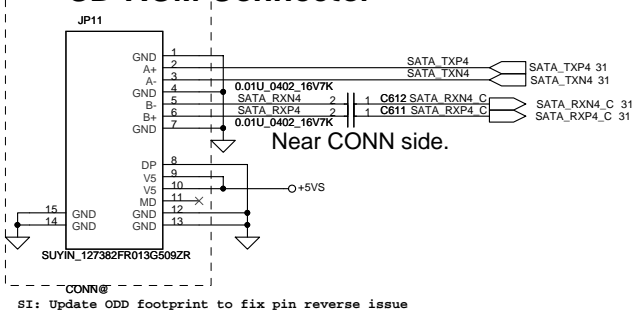
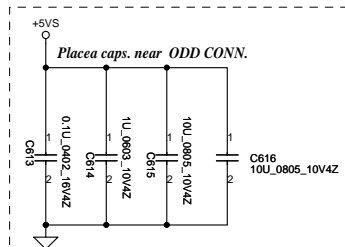
HDD Connector



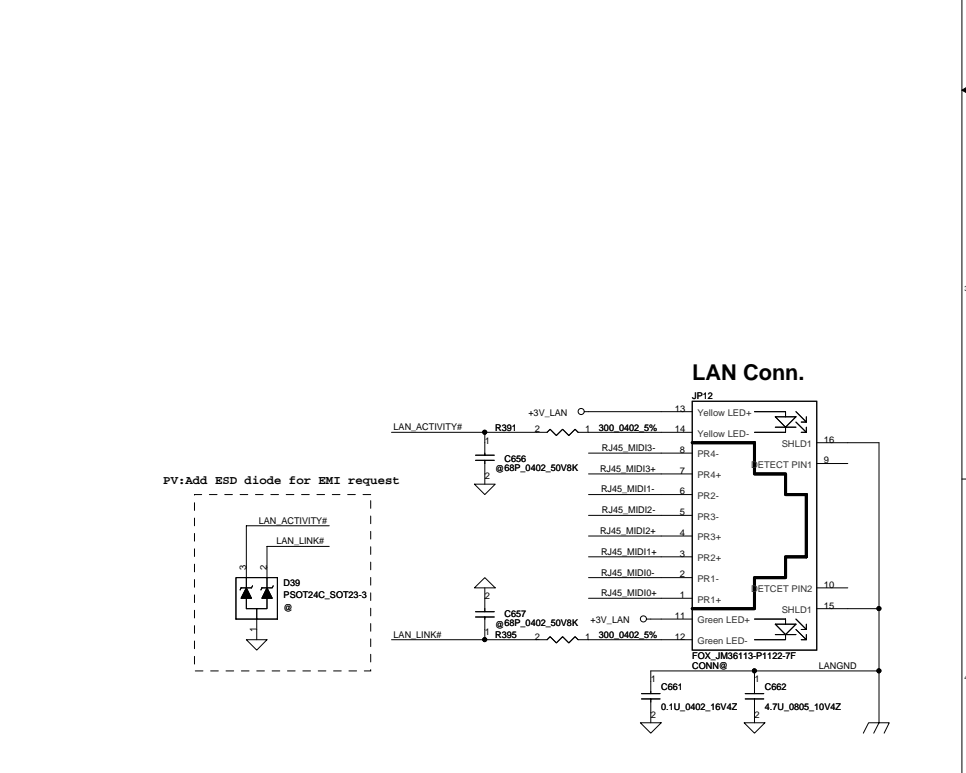
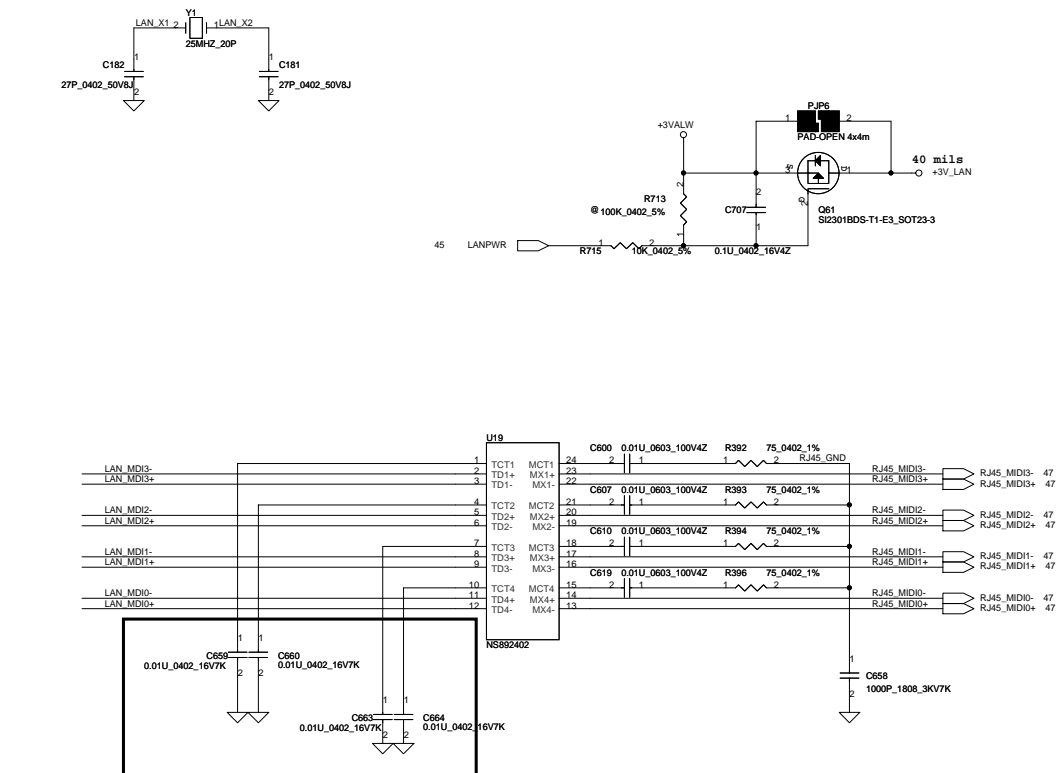
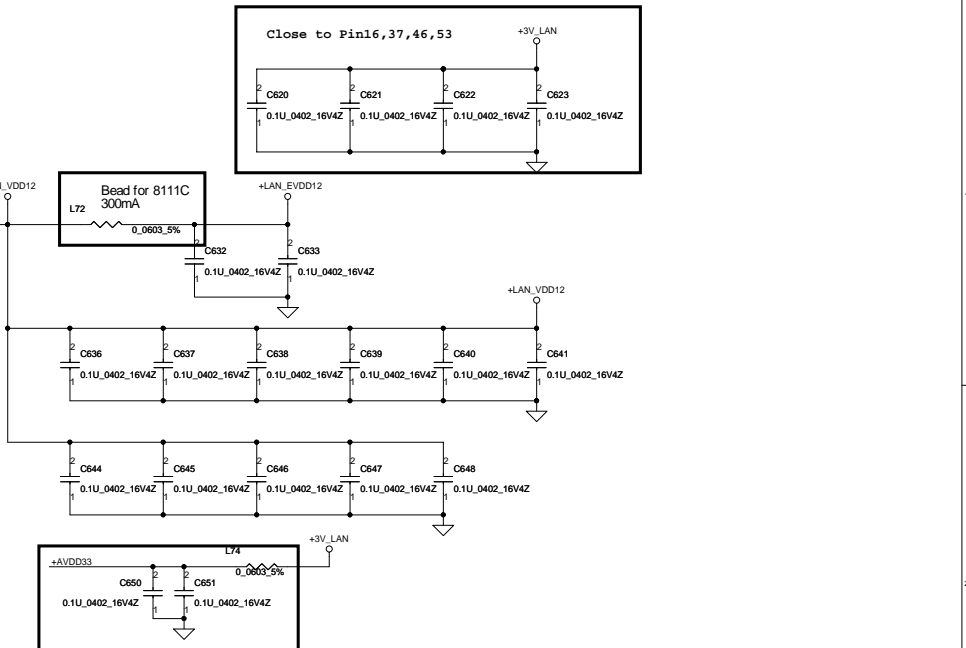
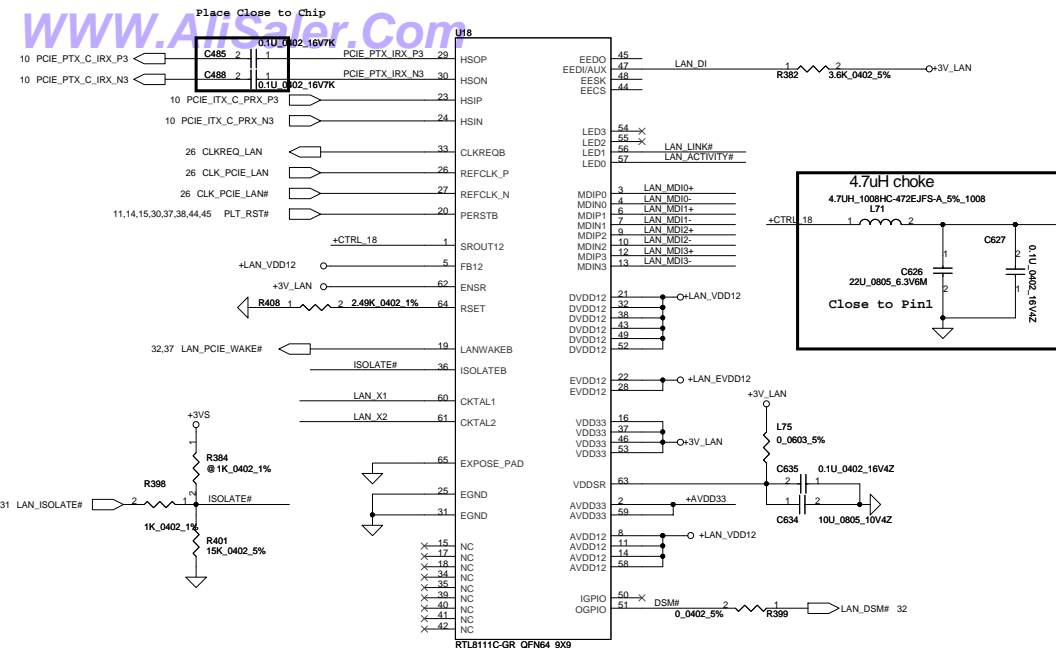
2nd HDD Connector-option



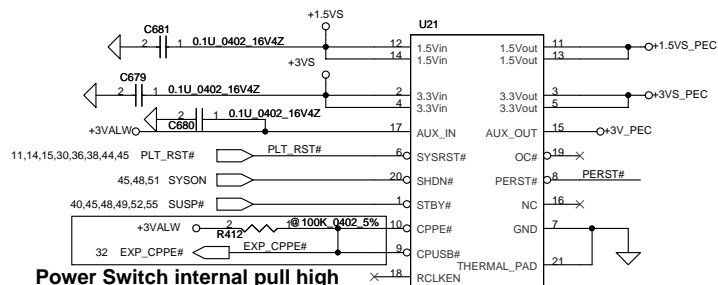
CD-ROM Connector



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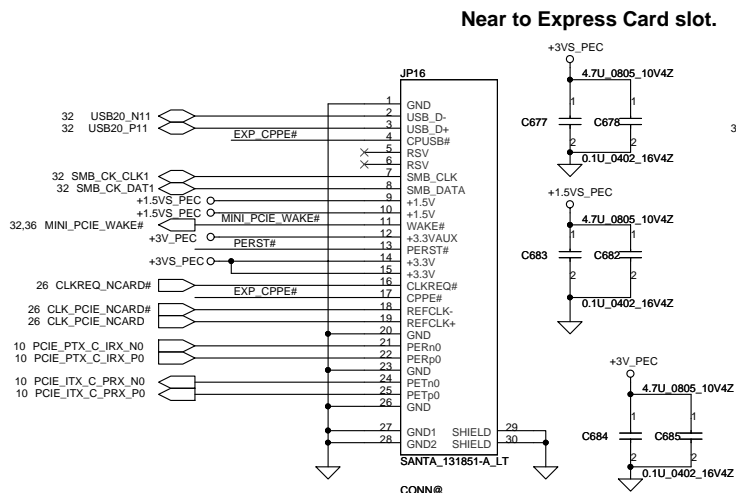
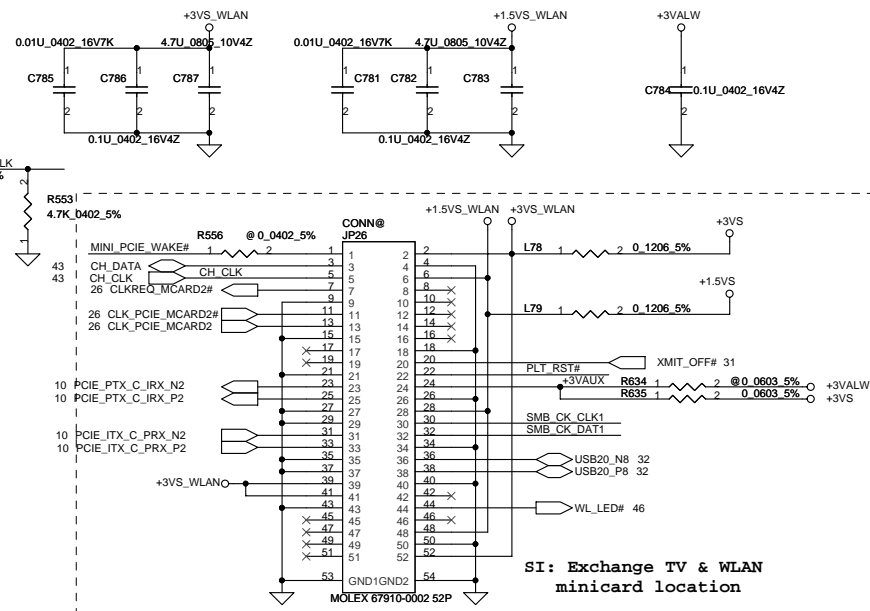


New Card



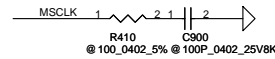
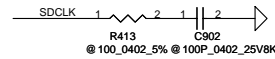
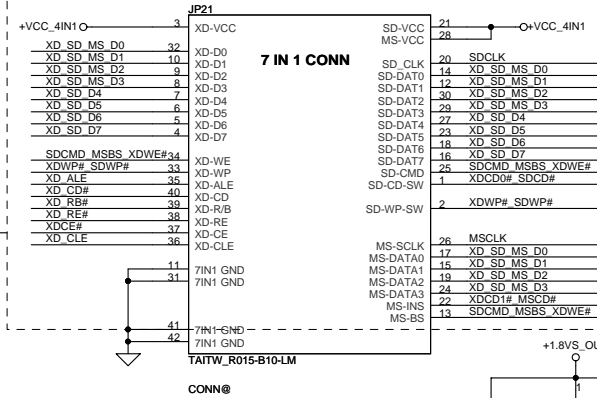
USE TI TPS2231MRGPR

Mini-Express Card---WLAN

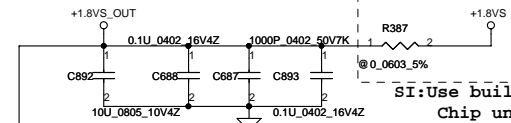


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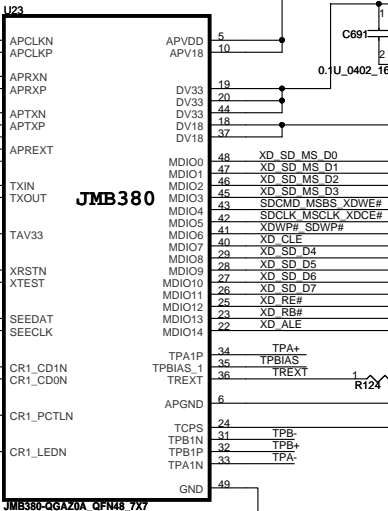
Card Reader Connector



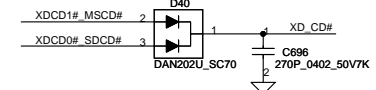
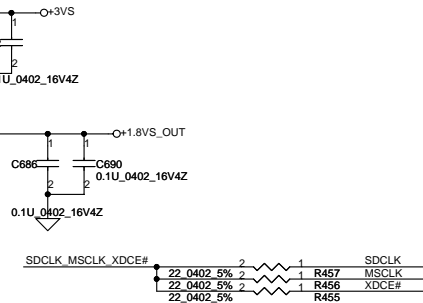
```
SI:Use build in Regulator
    Chip unmount R387
```



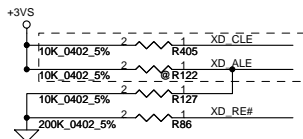
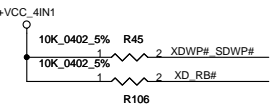
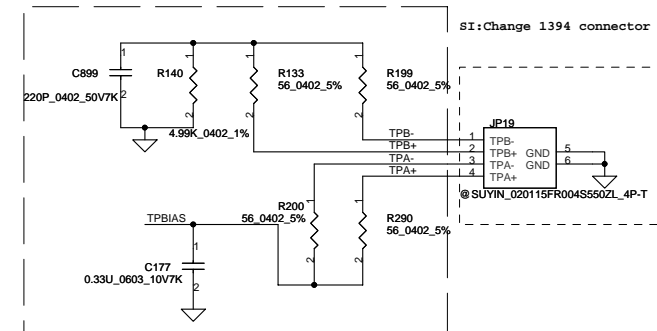
Power Circuit



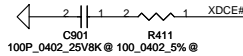
SI2: Use B version chip



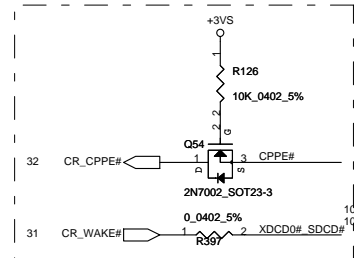
Close to Chip



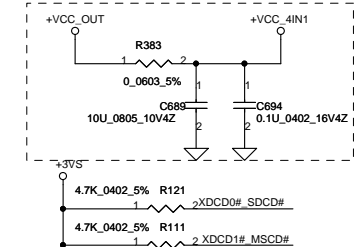
SI:Per Jmicro request change
R405 & R122 from 200K to 10K



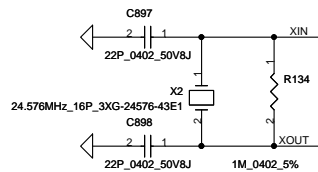
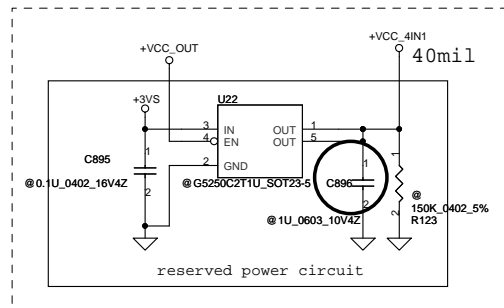
SI2:Support D3E function



SI:Use build in Regulator
Chip mount R383,C689,C694

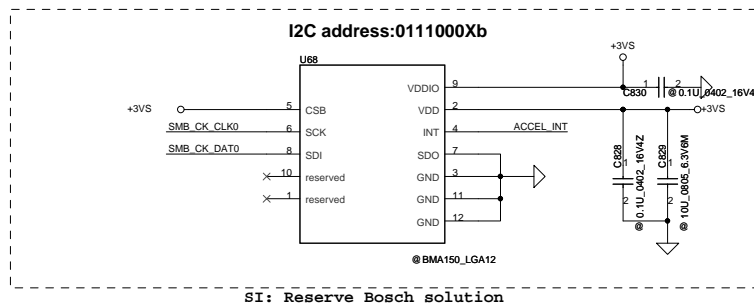
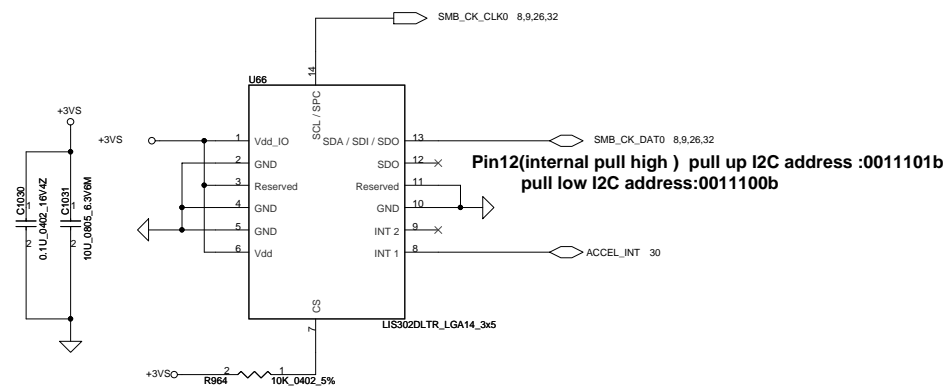


SI:Use build in Regulator High active control
Chip unmount U22 and relation parts



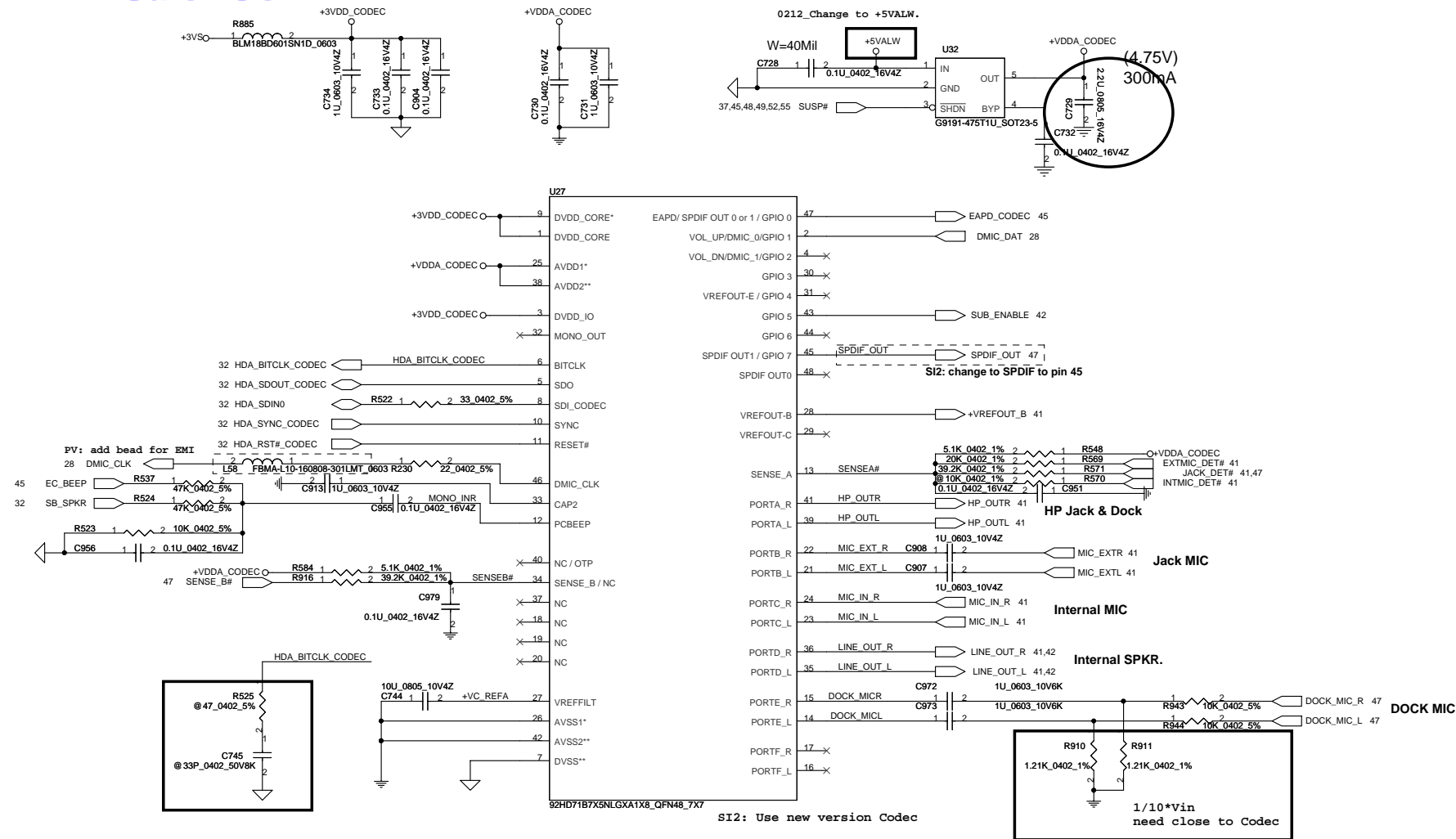
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ACCELEROMETER

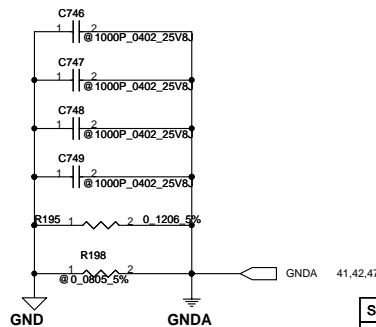


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CODEC POWER

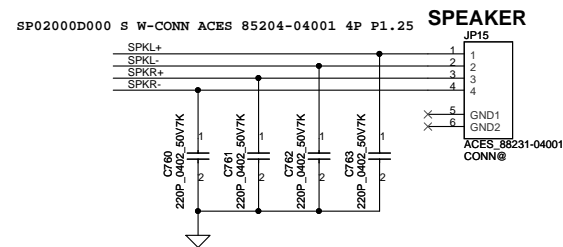
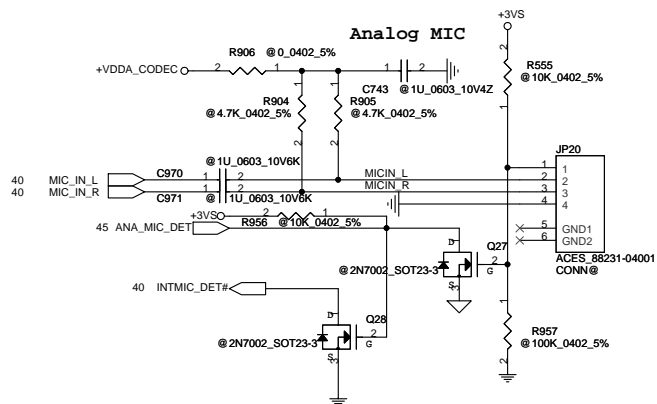
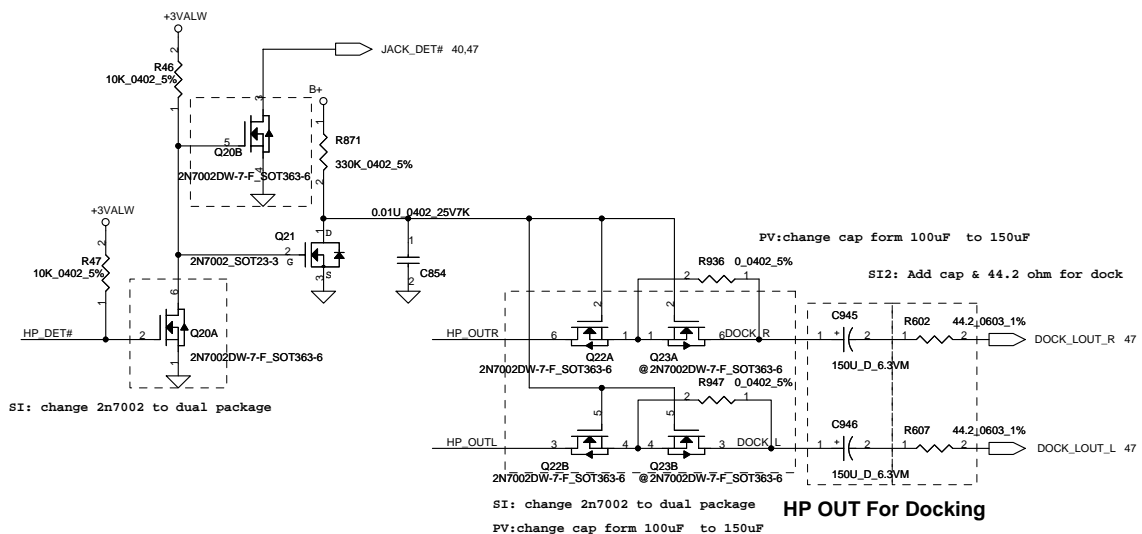
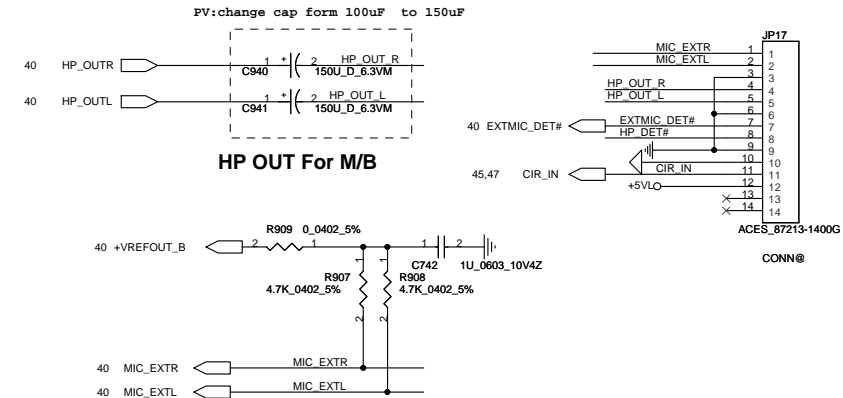
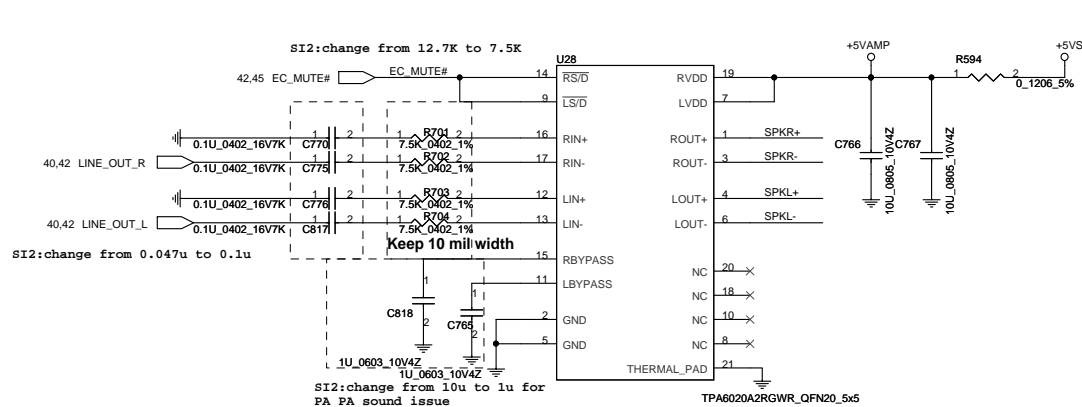


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



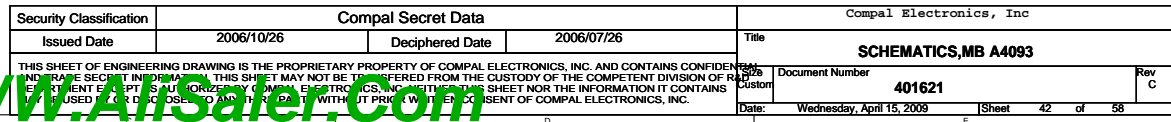
HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

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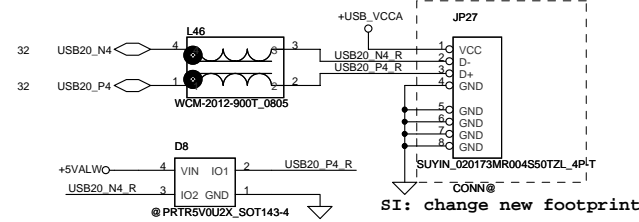
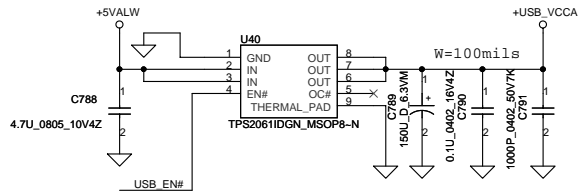


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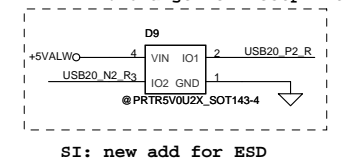
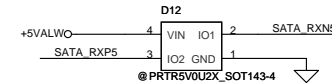
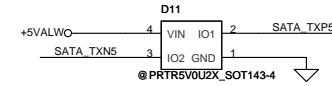
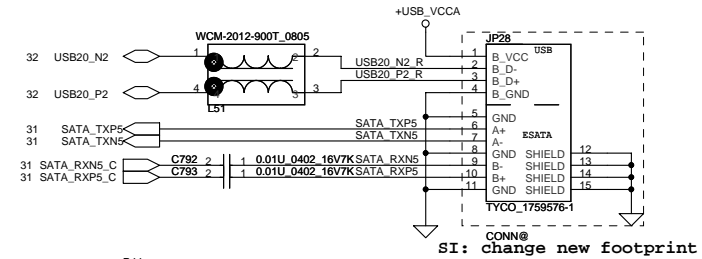
SCHEMATICS,MB A4093



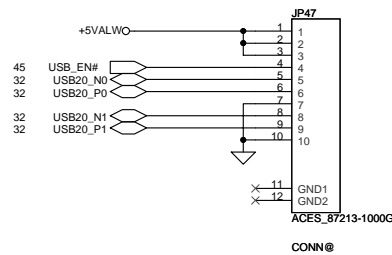
Left side USB CONNECTOR 0



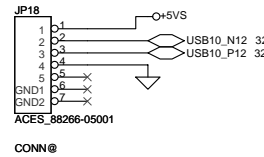
Left side ESATA/USB combination Connector



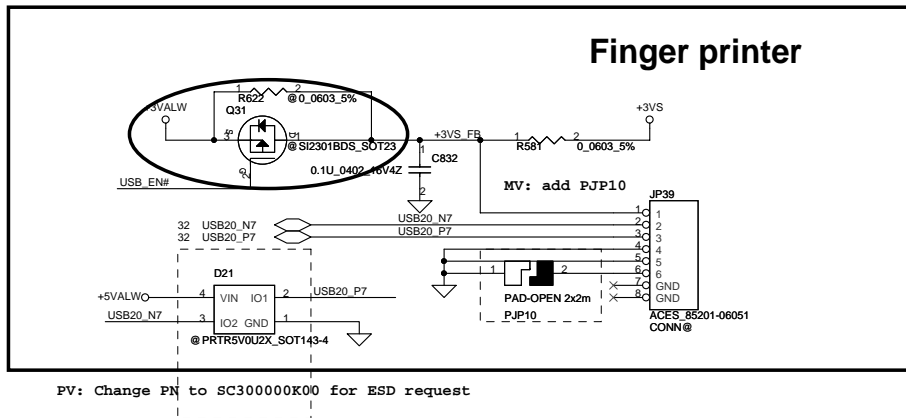
USB Board Conn



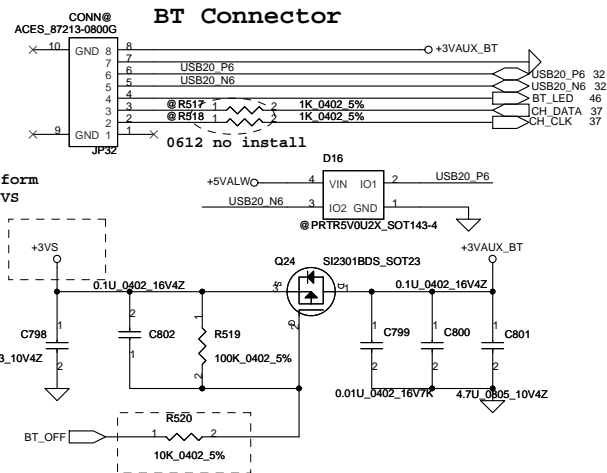
Touch screen



Finger printer

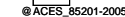


BT Connector

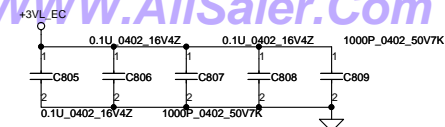


SI: change to 10K ohm to make sure MOS can turn on

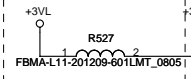
Security Classification			Compal Secret Data			Title		
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Rev	4	Document Number	401621	Rev C
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Date: Wednesday, April 15, 2009			Sheet 43 of 58			Schematics, MB A4093		



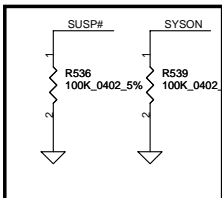
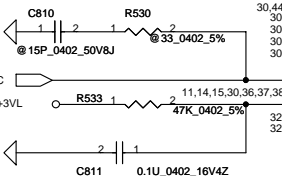
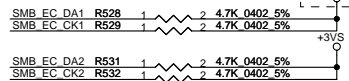
WWW.AllSale1.Com



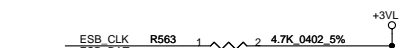
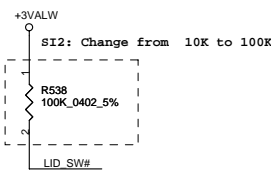
PV: change to BEAD for EMI request



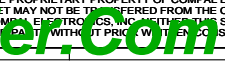
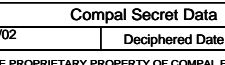
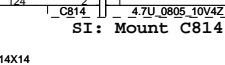
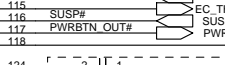
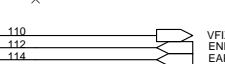
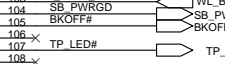
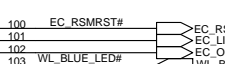
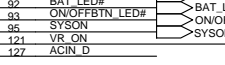
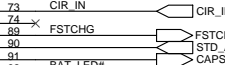
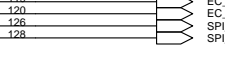
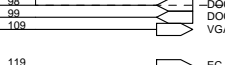
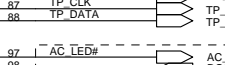
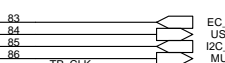
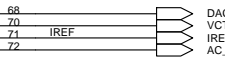
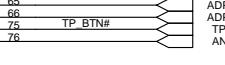
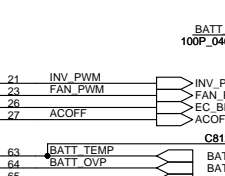
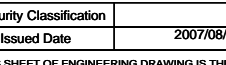
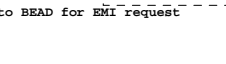
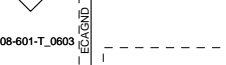
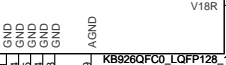
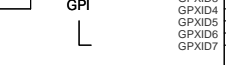
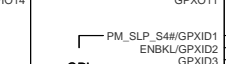
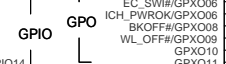
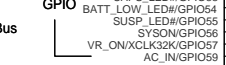
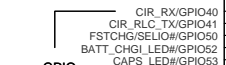
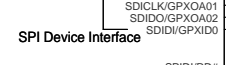
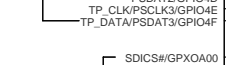
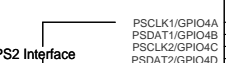
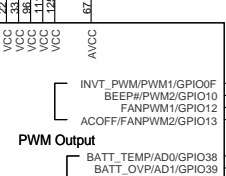
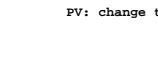
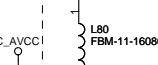
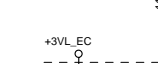
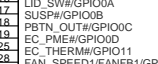
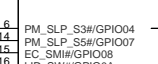
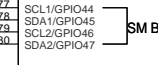
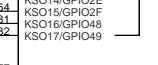
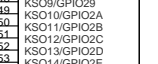
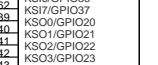
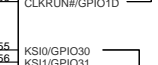
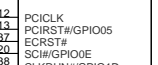
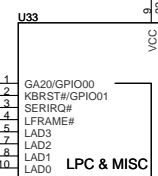
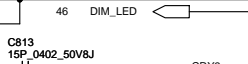
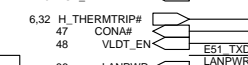
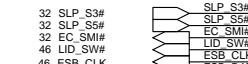
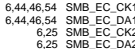
SI2: Change from +5V_L to +3V_L



0205 Add Pull down R402 for SUSP#.

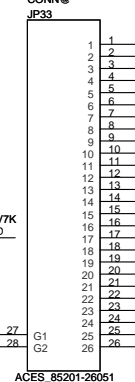


EC DEBUG port

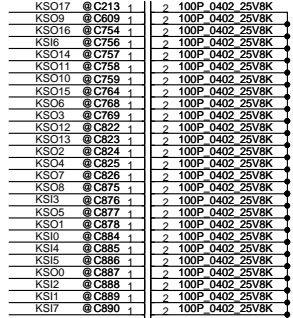


SI2: Change keyboard conn

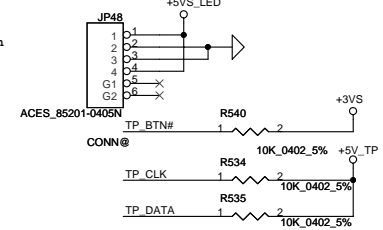
KBD CONN



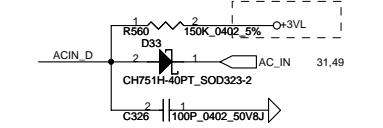
For EMI



KB Back Light Conn



PV: Change from +3VALW to +3V_L

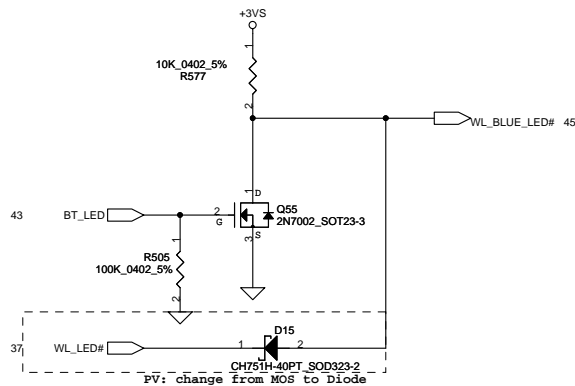
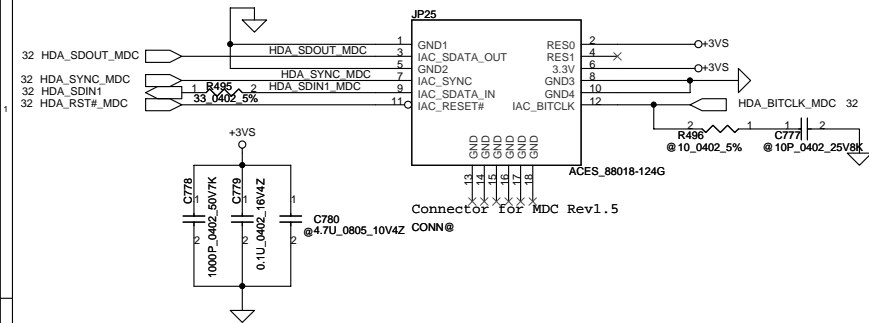


SI: Mount C814 for KB926C

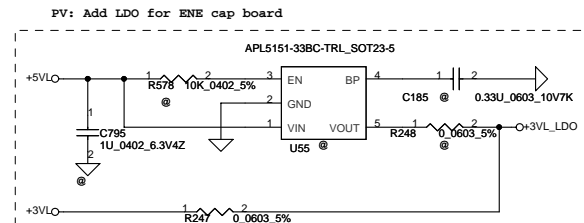
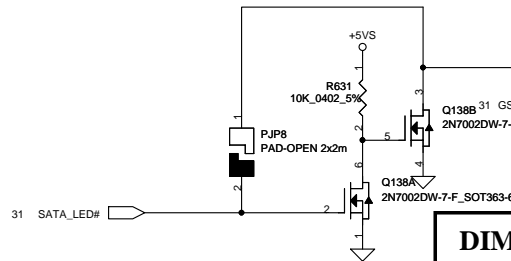
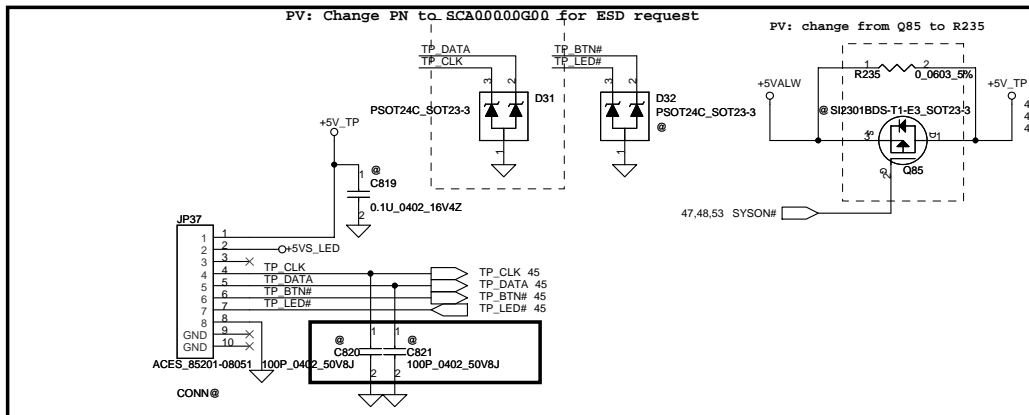


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				Customer	
				Date	Wednesday, April 15, 2009
				Sheet	45 of 58

Change type 4/25



T/P Board (Include T/P_ON/OFF)



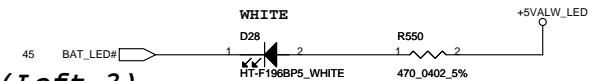
CAPS LOCK LED



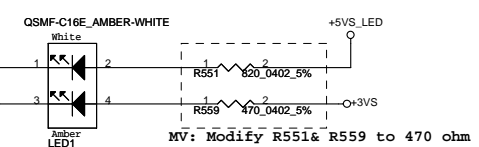
POWER LED(Left 1)



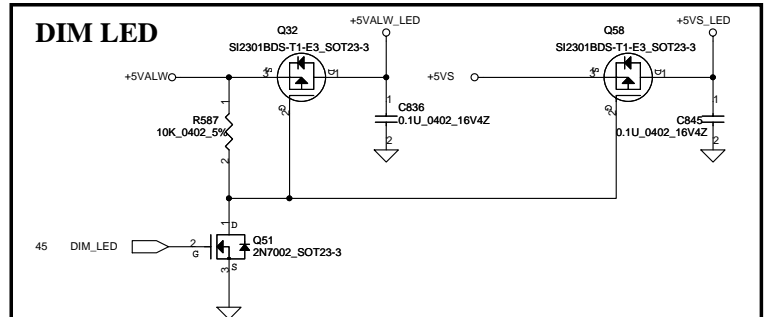
Battery Charge LED(Left 2)



HDD LED(Left 3)



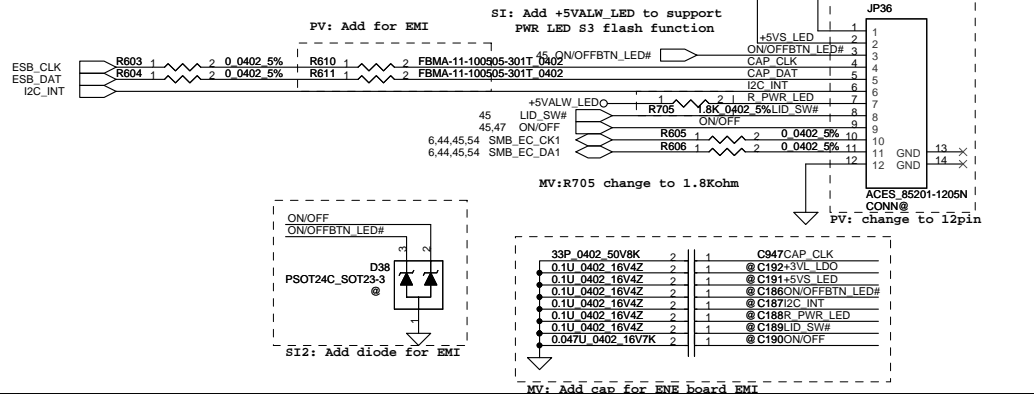
DIM LED



SI: Change to +3VL to support Qplay bottom boot in BATT mode

SWITCH BOARD.

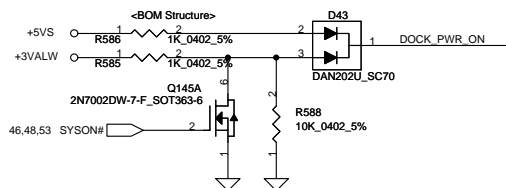
MV: Add cap for ENE board EMI



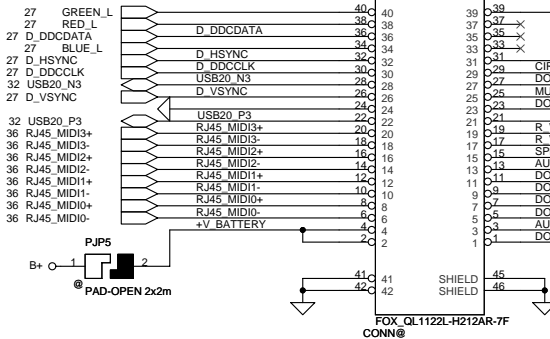
MV: Add cap for ENE board EMI

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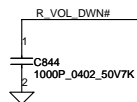
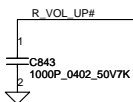
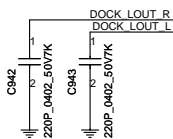
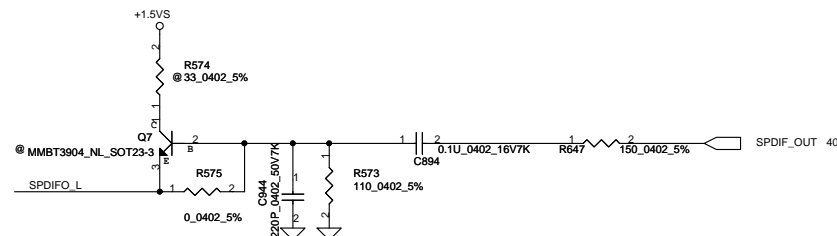
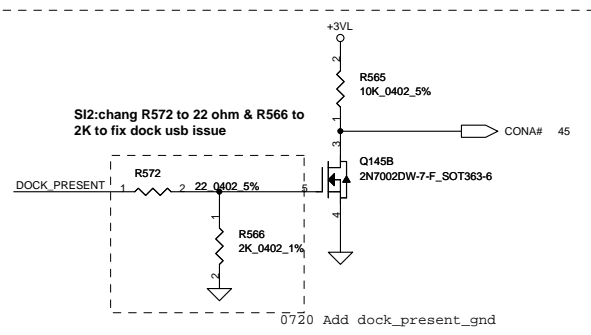
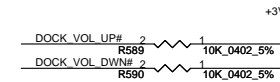
Atlas/ Saturn Dock



DOCK_PWR_ON Spec
 0V = Notebook S4/S5, Dock off
 2.5V = Notebook S3, Dock on
 4V = Notebook S0, Dock on

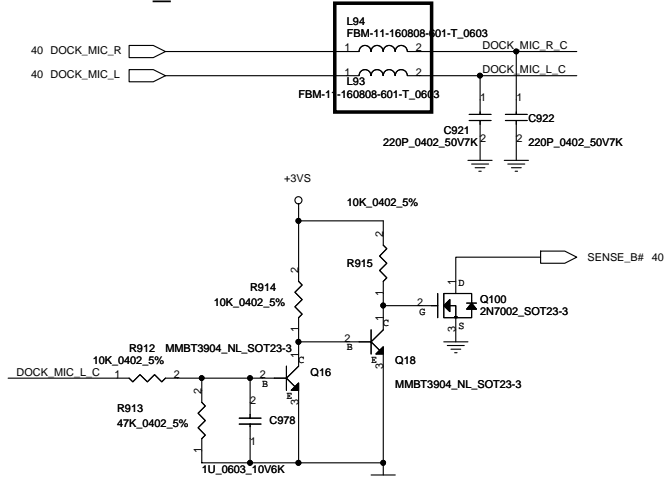


need change to reverse type connector



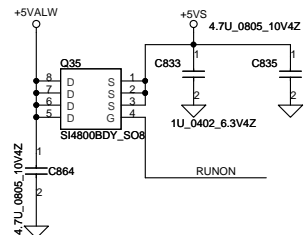
MIC_Dock

Need 600 Ohm 500 mA

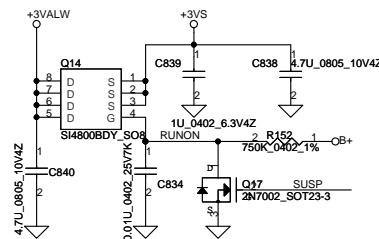


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				Date	Wednesday, April 15, 2009
				Sheet	47 of 58

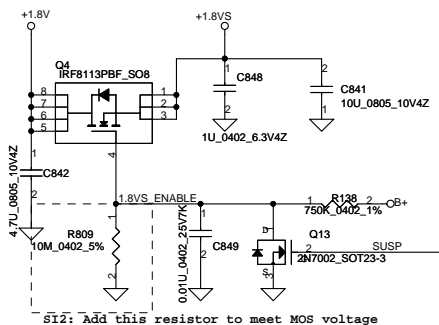
+5VALW TO +5VS



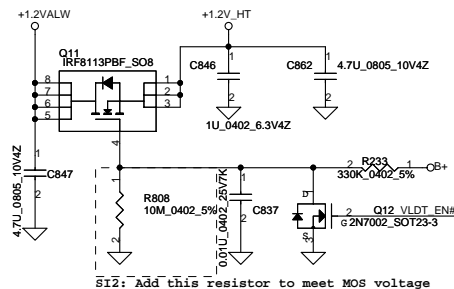
+3VALW TO +3VS



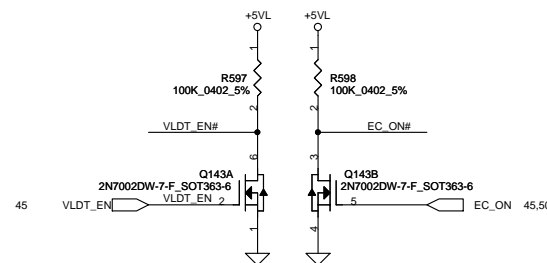
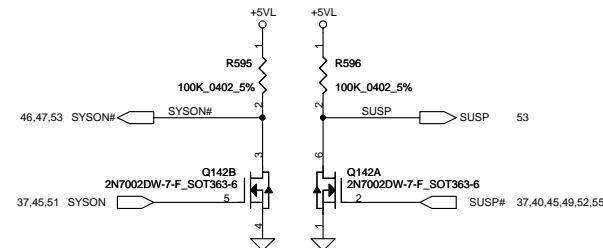
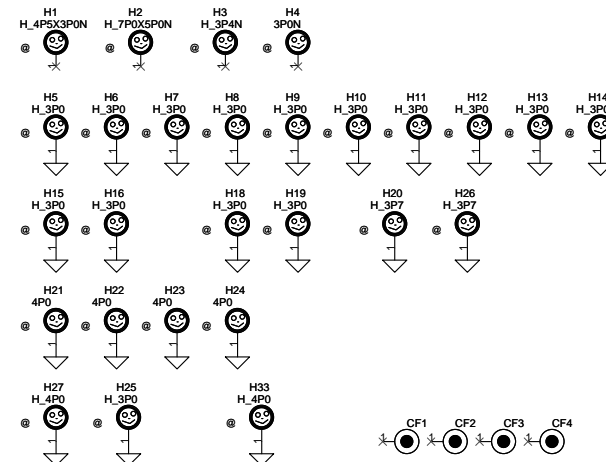
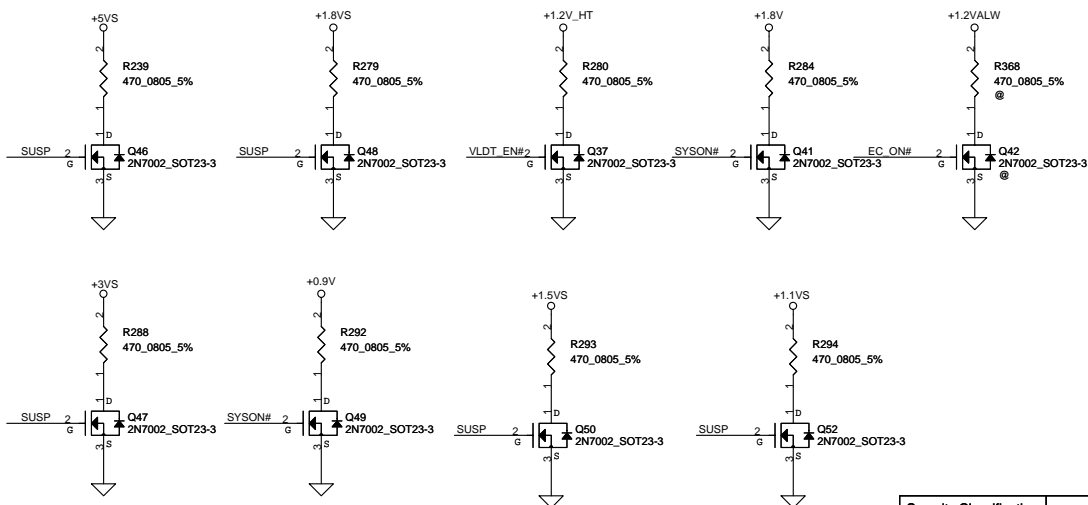
+1.8V TO +1.8VS



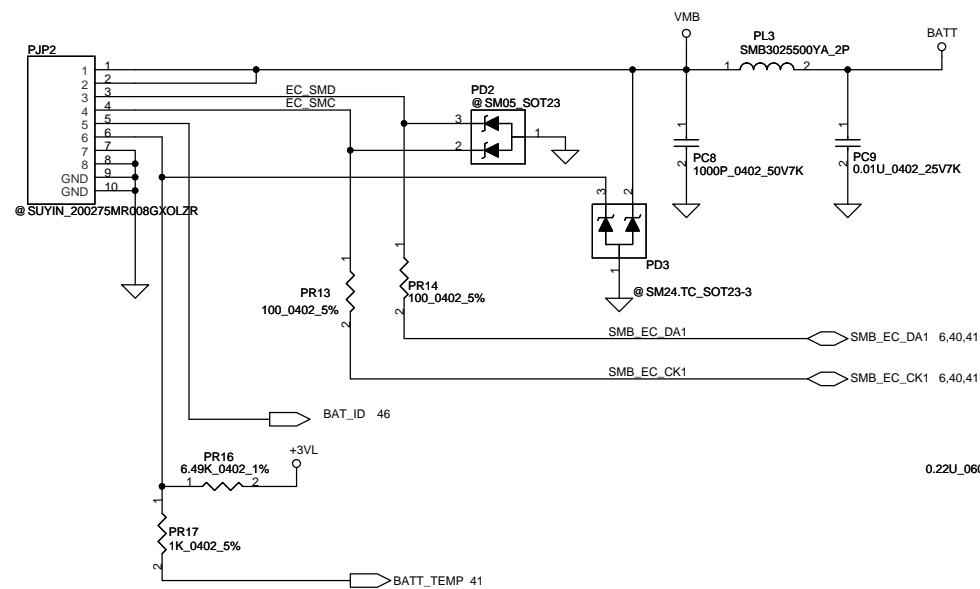
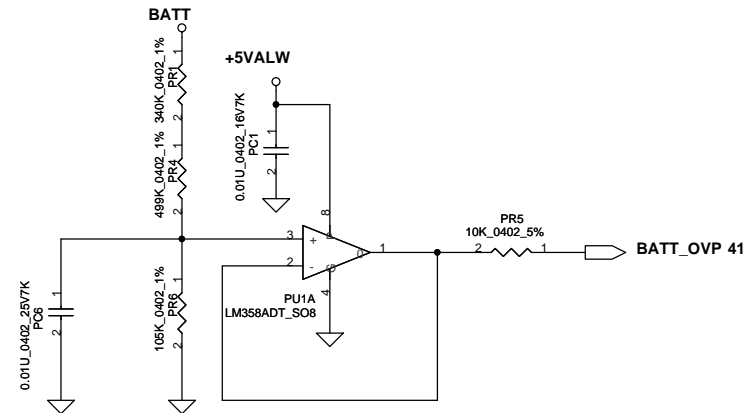
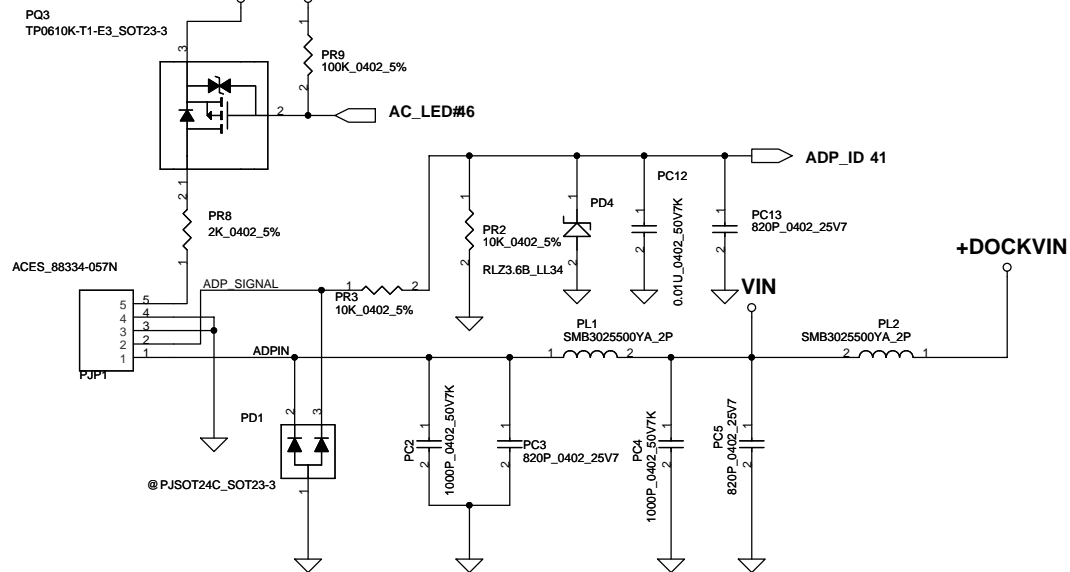
+1.2VALW TO +1.2V_HT



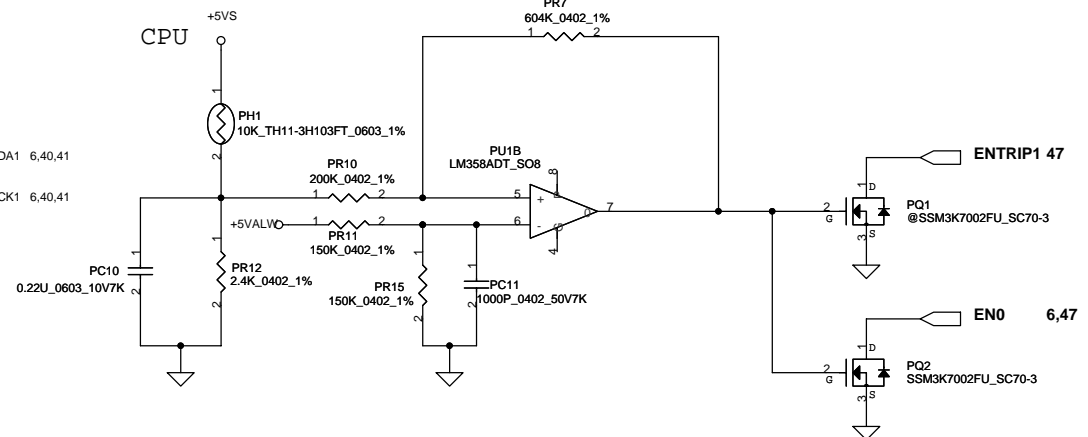
Discharge circuit



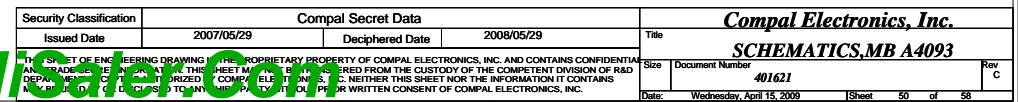
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				Deciphered Date				2008/08/02			
								SCHEMATICS, MB A4093			
								Document Number			
								401621			
								Rev			
								C			
								Date: Wednesday, April 15, 2009			
								Sheet 48 of 58			

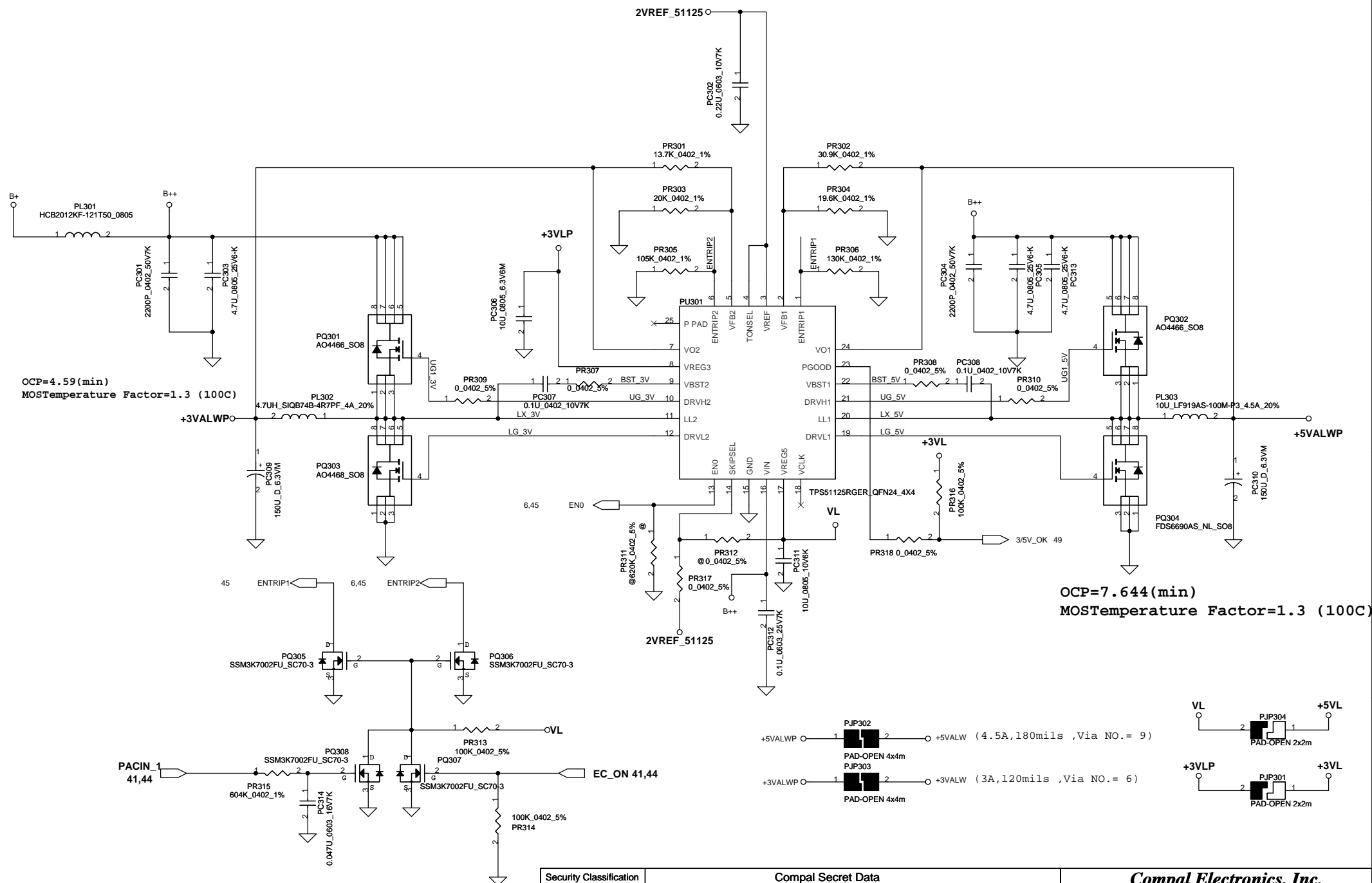


PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C

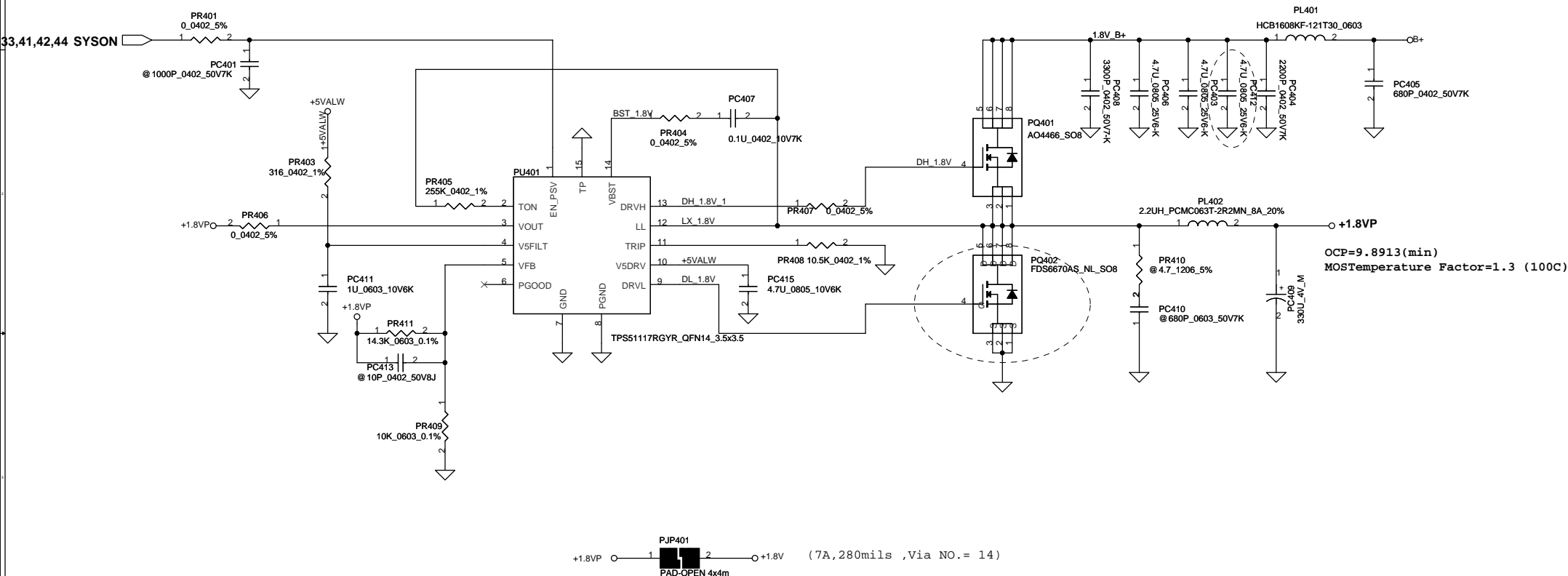


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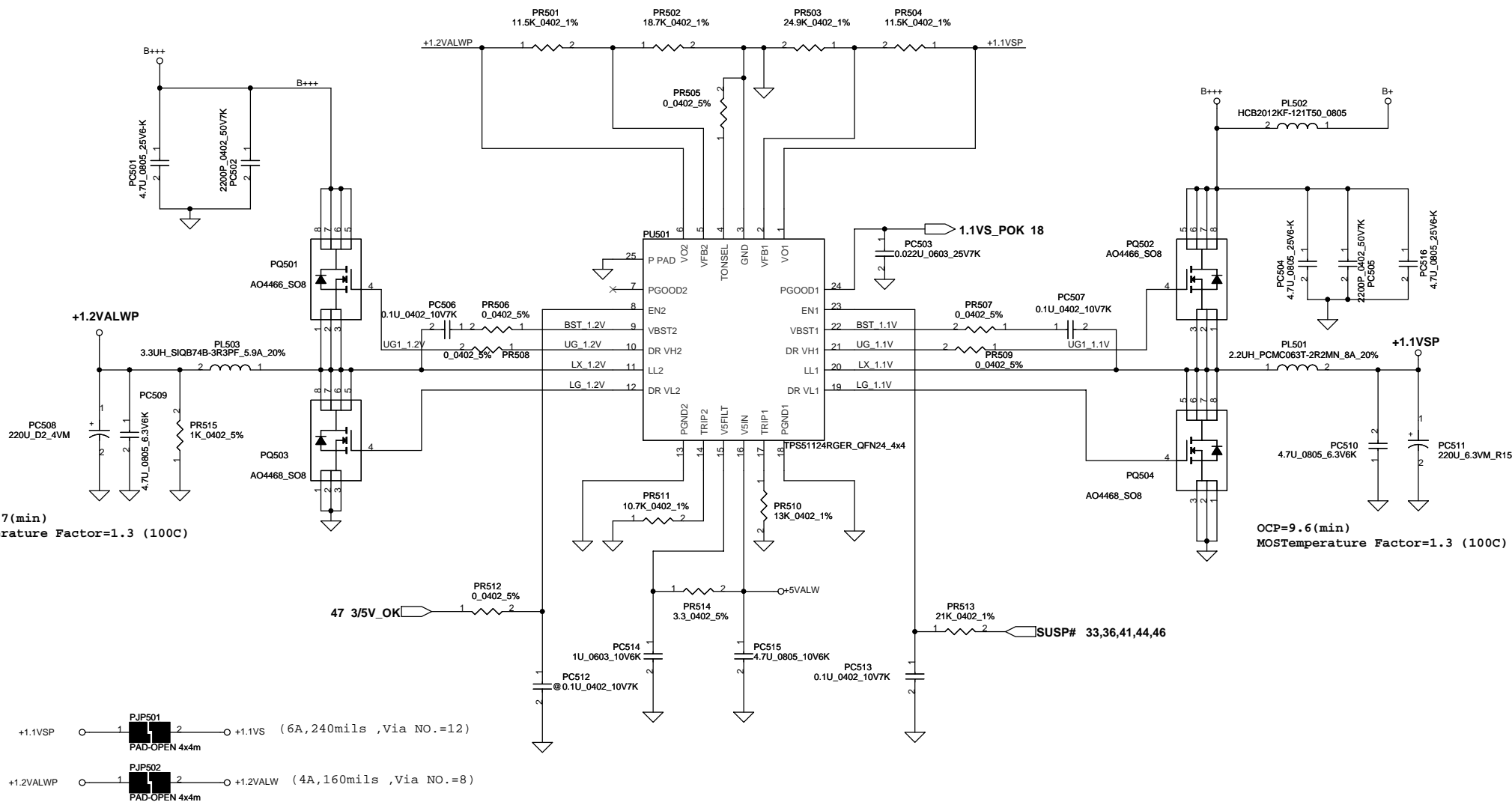
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				Date:	Wednesday, April 15, 2009		Sheet	51 of 58



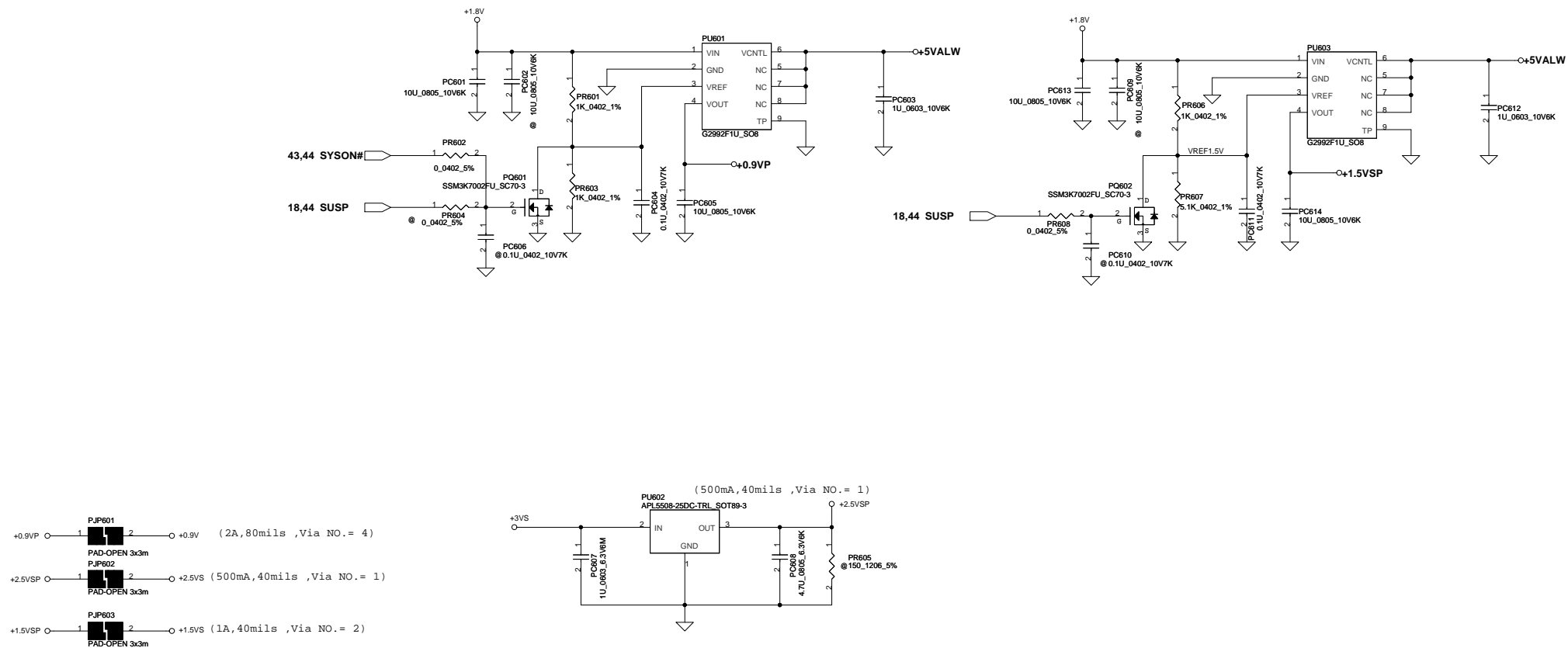
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Date:		Wednesday, April 15, 2009		Sheet	52 of 58

OCP=4.487(min)
MOSTemperature Factor=1.3 (100C)

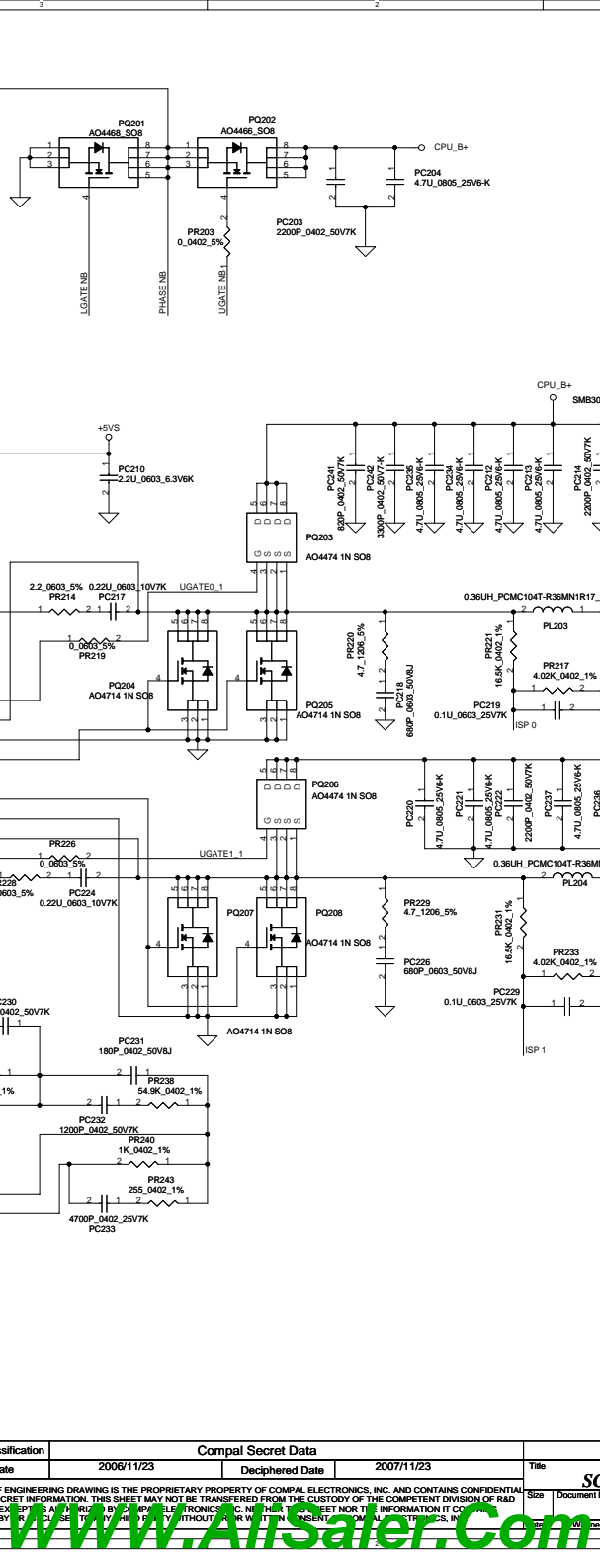
OCP=9.6(min)
MOSTemperature Factor=1.3 (100C)

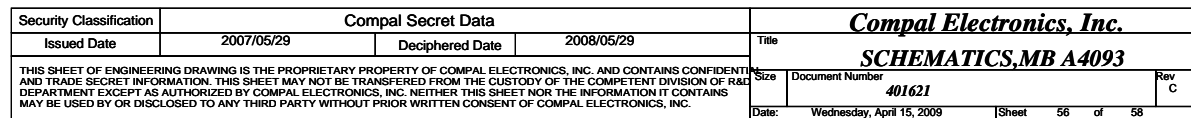


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Item	Modify List	PAGE	Fixed Issue and change item	M.B. Ver.
1	ADD *106,UV7,U7,U98,U8,U99,U9,UV10 (1000000V)	P15-P25	change M82S TO M86M	1.1
2	ADDQ9 (2M7002)	P15-P25	change M82S TO M86M	1.1
3	ADD QV3(S12301RD8)	P15-P25	change M82S TO M86M	1.1
4	ADD RV47(240 ohm)	P15-P25	change M82S TO M86M	1.1
5	ADD R42(0 ohm)	P15-P25	change M82S TO M86M	1.1
6	ADD RV19,RV44 (1K ohm)	P15-P25	change M82S TO M86M	1.1
7	ADD RV96,RV100,RV72,RV73,RV74,RV75,RV76,RV77,RV78,RV79,RV92,RV93,RV94,RV95,RV97,RV99,RV101,RV107,RV108,RV7,RV9,RV10,RV11,RV12,RV13,RV14,RV16,RV17,RV18,RV33,RV98,RV102(10K ohm)	P15-P25	change M82S TO M86M	1.1
8	ADD RV30,RV34(100K ohm)	P15-P25	change M82S TO M86M	1.1
9	ADD RV103,RV104,RV45,RV46,R403(4.7K ohm)	P15-P25	change M82S TO M86M	1.1
10	ADD RV36,RV37,RV38,RV39,RV40,RV41,RV42,RV43(100 ohm)	P15-P25	change M82S TO M86M	1.1
11	ADD RV6 (1.27Kohm)	P15-P25	change M82S TO M86M	1.1
12	ADD RV25,RV26,RV27,RV8(150 ohm)	P15-P25	change M82S TO M86M	1.1
13	ADD RV5(2K ohm)	P15-P25	change M82S TO M86M	1.1
14	ADD RV23,RV15,RV22(499 ohm)	P15-P25	change M82S TO M86M	1.1
15	ADD RV60,RV61,RV62,RV63,RV66,RV67,RV68,RV69,RV54,RV55,RV56,RV57,RV48,RV49,RV50,RV51(4.99K ohm)	P15-P25	change M82S TO M86M	1.1
16	ADD RV24(715 ohm)	P15-P25	change M82S TO M86M	1.1
17	ADD RV28(75 ohm)	P15-P25	change M82S TO M86M	1.1
18	ADD YV1(CRYSTAL 27MHz)	P15-P25	change M82S TO M86M	1.1
19	ADD RV103,RV104,RV45,RV46,R403(4.7K ohm)	P15-P25	change M82S TO M86M	1.1
20	ADD LV1, LV2, LV3, LV4, LV5, LV6, LV7, LV8, LV9, LV10, LV11, LV12, LV13, LV14, LV15, LV16, LV17, LV18, LV19, LV21, LV22, LV23, LV24, LV25 (MURATA BLM18P0121SN10)	P15-P25	change M82S TO M86M	1.1
21	ADDCV226,CV227,CV234,CV235,CV249,CV250,CV257,CV258,CV203,CV204,CV211,CV212,CV180,CV181,CV188,CV189,CV42,CV45,CV48,CV52,CV53,CV56,CV59,CV64,CV67,CV68,CV71,CV76,CV84,CV85,CV90,CV92,CV95,CV97,CV99,CV101,CV108, CV117,CV119,CV131,CV132,CV136,CV140,CV145,CV149,CV157,CV165,CV166,CV169,CV173(10u)	P15-P25	change M82S TO M86M	1.1
22	ADD CV80,CV444,CV229,CV230,CV231,CV232,CV237,CV238,CV239,CV240,CV242,CV246,CV247,CV252,CV253,CV254,CV255,CV260,CV261,CV262,CV263,CV265,CV267,CV269,CV270,CV206,CV207,CV208,CV209,CV214,CV215,CV216, CV217,CV219,CV221,CV223,CV224,CV236,CV183,CV184,CV185,CV186,CV191,CV192,CV193,CV194,CV198,CV200,CV201,CV44,CV46,CV49,CV50,CV55,CV58,CV60,CV62,CV66,CV69,CV72,CV75,CV79,CV83, CV87,CV88,CV106,CV114,CV120,CV125,CV159,CV168,CV171,CV172,CV175,CV176,CV177,CV178,CV179,CV272(0.1u)	P15-P25	change M82S TO M86M	1.1
23	ADD CV77,CV78(22P)	P15-P25	change M82S TO M86M	1.1
24	ADD CV73 (2200P)	P15-P25	change M82S TO M86M	1.1
25	ADDCV233,CV241,CV256,CV264,CV210,CV218,CV187,CV195(0.010)	P15-P25	change M82S TO M86M	1.1
26	ADD CV245,CV228,CV236,CV243,CV261,CV269,CV46,CV68,CV205,CV213,CV220,CV222,CV197,CV282,CV180,CV189,CV41,CV43,CV47,CV51,CV57,CV63,CV65,CV70,CV73,CV74,CV82,CV86,CV89,CV93,CV96,CV98,CV100,CV103,CV104, CV105,CV107,CV109,CV111,CV118,CV121,CV135,CV139,CV144,CV162,CV163,CV164,CV54,CV61,CV94,CV102,CV110,CV112,CV115,CV116,CV123,CV124,CV126,CV127,CV129,CV130,CV133,CV134,CV137,CV138,CV141,CV142, CV146,CV147,CV150,CV151,CV153,CV154,CV155,CV156,CV158,CV160,CV161,CV167,CV170,CV174(75 ohm) ADD RV28(10)	P15-P25	change M82S TO M86M	1.1
27	ADD CV9,CV10,CV11,CV12,CV13,CV14,CV15,CV16,CV17,CV18,CV19,CV20,CV21,CV22,CV23,CV24,CV25,CV26,CV27,CV28,CV29,CV30,CV31,CV32,CV33,CV34,CV35,CV36,CV37,CV38,CV39,CV40 (0.10)	P15-P25	change M82S TO M86M	1.1
28	ADD CV122,CV91,CV128(3300)	P15-P25	change M82S TO M86M	1.1
PV				
1	Change RV30 100K to 100 ohm	P16	About GBU 27MHz	
2	Change PR702 4.7K to 0 ohm	P55	About GBU JV delay time	
3	del PC702 0.1 u	P55	About GBU JV delay time	
4	change NET_QMA44 TO U8 P3 pin	P22	about GBU A channel VRAM	
5	change NET_QMA45 TO U8 B3 pin	P22	about GBU A channel VRAM	
6	Change NET_QSA4_QSA44 TO U8 P7,B8 PIN	P22	about GBU A channel VRAM	
7	Change NET_QSA5_QSA5TO U8 B7,A8 PIN	P22	about GBU A channel VRAM	
8	change NET_QMA47 TO U8 P3 pin	P22	about GBU A channel VRAM	
9	change NET_QMA45 TO U8 B3 pin	P22	about GBU A channel VRAM	
10	change NET_QSA7_QSA7TO U8 P7,B8 PIN	P22	about GBU A channel VRAM	
11	Change NET_QSA6_QSA6 TO U8 B7,A8 PIN	P22	about GBU A channel VRAM	
12	Change UV12 BOM SA010320120 to SA010320110	P25	about GBU Thermal Sensor	
13	Modify_R237,R238,R176,R209_PULL +3VS TO +3VS_DELAY	P27_P28	Change power plan	
14	ADD LV20,CV152,CV148,CV143	P18	ADD M86M +VDDM5 POWER	